UNIT - 1
BASICS OF OPERATIONAL AMPLIFIERS

PART-A

1. **Define an Integrated circuit.**
   An integrated circuit(IC) is a miniature, low cost electronic circuit consisting of active and passive components fabricated together on a single crystal of silicon. The active components are transistors and diodes and passive components are resistors and capacitors.

2. **Mention the advantages of integrated circuits over discrete components. (May 2010)**
   - Miniaturization and hence increased equipment density.
   - Cost reduction due to batch processing.
   - Increased system reliability due to the elimination of soldered joints.
   - Improved functional performance.
   - Matched devices. *Increased operating speeds.
   - Reduction in power consumption.

3. **What is active load? Where it is used and why?**
   (MAY/JUNE 2010)
   The active load realized using current source in place of the passive load in the collector arm of differential amplifier makes it possible to achieve high voltage gain without requiring large power supply voltage.

4. **Why open loop OP-AMP configurations are not used in linear applications? (May/June 2010)**
   The open loop gain of the op-amp is not a constant and it varies with changing the temperature and variations in power supply. Also the bandwidth of the open loop op-amp is negligibly small. For this reasons open loop OP-AMP configurations are not used in linear applications.

5. Write Ideal OPAMP Characteristics.

1) Open loop voltage gain, AoL=∞.

2) Input Impedance , Ri=∞.

3) Output impedance, Ro=0.

4) Bandwidth, BW=∞.

5) Zero offset, i.e. Vo=0 when V1=V2=0.

6) Slew rate=∞.

7) Output should not change when temperature changes.

6. Define Ripple Rejection Ratio.

The ability of circuit to reject input ripples and an indication of how much ripples are present at the output due to input is given by the factor ripple rejection ratio.

RRR=20[Vri/Vro].

7. Define virtual ground of a OP-Amp? (May/June 2010)

A virtual ground is a ground which acts like a ground. It is a point that is at the fixed ground potential (0v),though it is not practically connected to the actual ground or common terminal of the circuit.

8. Define input offset current. State the reasons for the offset currents at the input of the op-amp.

The difference between the bias currents at the input terminals of the op-amp is called as input offset current. The input terminals conduct a small value of dc current to bias the input transistors. Since the input transistors cannot be made identical, there exists a difference in bias currents.

9. Define CMRR of an op-amp. (DEC 09)

The relative sensitivity y of an op-amp to a difference signal as compared to a common mode signal is called the common –mode rejection ratio. It is expressed in decibels.

CMRR= Ad/Ac

10. What are the applications of current sources?

Transistor current sources are widely used in analog ICs both as biasing elements and as load devices for amplifier stages.

11. Justify the reasons for using current sources in integrated circuits.

(i) Superior insensitivity of circuit performance to power supply variations and temperature.

(ii) More economical than resistors in terms of die area required to provide bias currents of small value.

(iii) When used as load element, the high incremental resistance of current source results in high voltage gains at low supply voltages.

12. What is the advantage of widlar current source over constant current source?

Using constant current source output current of small magnitude (microamp range) is not attainable due to the limitations in chip area. Widlar current source is useful for obtaining small output currents. Sensitivity of widlar current source is less compared to constant current source.

13. Mention the advantages of Wilson current Source.

(i) Provides high output resistance.

(ii) Offers low sensitivity to transistor base currents.

14. Define sensitivity.

Sensitivity is defined as the percentage or fractional change in output current per percentage or fractional change in power-supply voltage.

15. What are the limitations in a temperature compensated zener-reference source?

A power supply voltage of atleast 7 to 10 V is required to place the diode in the breakdown region and that substantial noise is introduced in the circuit by the avalanching diode.

16. In practical op-amps, what is the effect of high frequency on its performance?

The open-loop gain of op-amp decreases at higher frequencies due to the presence of parasitic capacitance. The closed-loop gain increases at higher frequencies and leads to instability.

17. What is the need for frequency compensation in practical op-amps?

Frequency compensation is needed when large bandwidth and lower closed loop gain is desired. Compensating networks are used to control the phase shift and hence to improve the stability.

18. Define slew rate. (MAY 2010)(April/May 2015)

The slew rate is defined as the maximum rate of change of output Voltage caused by a step input voltage. An ideal slew rate is infinite which means that op-amp's output voltage should change instantaneously in response to input step voltage.

19. Why IC 741 is not used for high frequency applications?

IC741 has a low slew rate because of the predominance of capacitance present in the circuit at higher frequencies. As frequency increases the output gets distorted due to limited slew rate.

20. What causes slew rate? (DEC 09)

There is a capacitor with-in or outside of an op-amp to prevent oscillation. The capacitor which prevents the output voltage from responding immediately to a fast changing input.

21. What happens when the common terminal of V^+ and V^- sources is not grounded? (DEC 09)

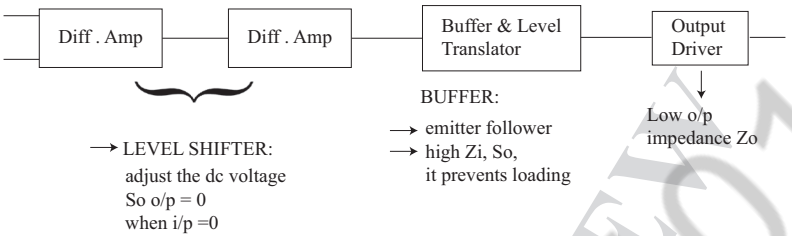
If the common point of the two supplies is not grounded, twice the supply voltage will get applied and it may damage the op-amp.

22. Define input offset voltage.

A small voltage applied to the input terminals to make the output voltage as zero when the two input terminals are grounded is called input offset voltage.

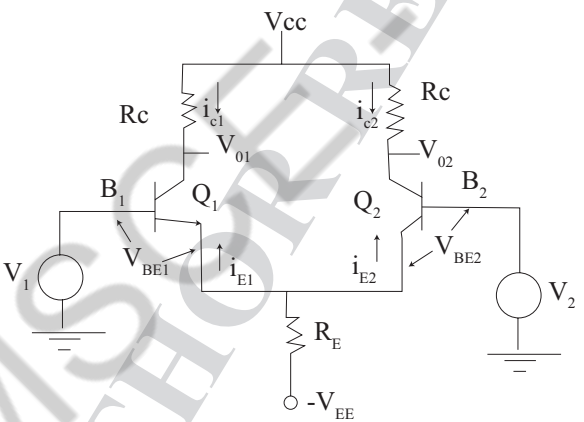
PART-B

1. Explain the Internal blocks of Operational Amplifier. (May 2015)



Output voltage should swing symmetrically with respect to ground. S_o the amplifier is provided with both positive and negative power supply.

DIFF. Amp: OPAMP Internal Circuit



It should provide high gain to the difference signal and cancel the common mode signal.

Sensitivity of an output amp of difference mode signal to common mode signal is called CMRR.

CMRR should be high. Input impedance also should be high.

D_c amplifies

I_{CBO}, V_{BE}, h_{FE} are dependent on temperature. S_o operating point will get drifted.

This problem can be eliminated by using diff amp.

This circuit has low drift because of symmetrical construction.

B_1 = '+' input terminal

B_2 = '–' input terminal

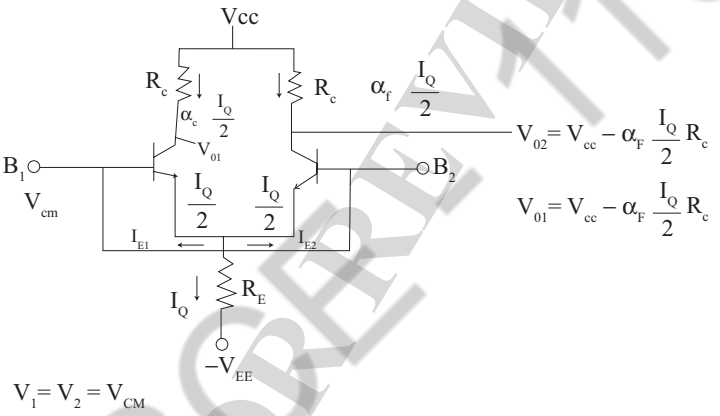
4 types of configuration

(i) Difference input, difference output

(ii) Difference input, single ended output

(iii) Single input, difference output

(iv) Single input, single ended output



Since the two transistors are matched and due to symmetrical construction, I_Q divides equally through transistors Q_1 & Q_2.

ie $$i_{E1} = i_{E2} = \frac{I_Q}{2}$$

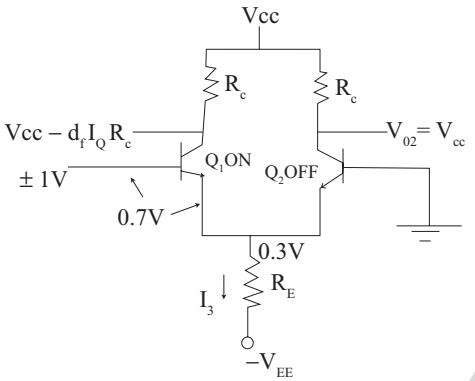
Thus $$i_{c1} = i_{c2} = \alpha_F \frac{I_Q}{2}$$

$$V_{o1} = V_{cc} - \alpha_F \frac{I_Q}{2} R_c$$

$$V_{o2} = V_{cc} - \alpha_F \frac{I_Q}{2} R_c$$

$$V_o = V_{o1} - V_{o2} = 0$$

Even if we change V_{CM}, voltage across collectors will not change. Thus the differential pair does not respond to common mode signal.



When $V_1 = 1V$, $V_2 = 0$, entire current I_Q flows through Q_1

S_o $V_{01} = Vcc - \propto_F I_Q R_C$ $V_{02} = Vcc$ $V_E = 0.3V$

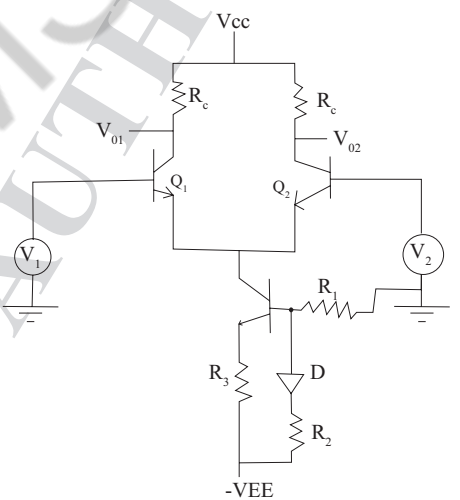
When $V_1 = -1V$, $V_2 = 0V$, entire current flows through Q_2

S_o, $V_{01} = Vcc$, $V_{02} = Vcc - \propto_F I_Q R_C$

Thus the differential pair responds only to differential signal not common mode signal

Circuits for Improving CMRR:

For high value of CMRR, R_E should be large. R_E has some limitations, ie if we increase R_E, V_{EE} have to be decreased. Then operating current increases, h_{ie} decreases , h_{fe} decreases and CMRR decreases. To overcome that problem, constant current bias is used in place of R_E.



Apply KVL,

$$I_Q \simeq I_3 = \frac{1}{R_3}\left(V_D + (V_{EE} - V_D)\frac{R_2}{R_1 + R_2} - V_{BE3}\right)$$

$$I_Q \simeq I_3 = \frac{1}{R_3}\left(V_D + V_{EE}\frac{R_2}{R_1 + R_2} - V_D\frac{R_2}{R_1 + R_2} - V_{BE3}\right)$$

$$I_Q \simeq I_3 = \frac{1}{R_3}\left(V_D + \frac{R_1}{R_1 + R_2} + V_{EE}\frac{R_2}{R_1 + R_2} - V_{BE3}\right)$$

By proper choice of resistors R_1 & R_2

$$V_{BE3} = V_D\frac{R_1}{R_1 + R_2}$$

$$I_Q \simeq I_3 = \frac{1}{R_3}\left(V_{EE}\frac{R_2}{R_1 + R_2}\right)$$

I_Q independent of V_1 and V_2

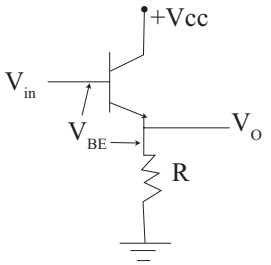
Diode D makes I_Q, temperature independent .ie V_{BE3} decreases if temp is increased, Diode also has temperature dependence. So these two variations will get cancelled. Since I_Q is constant, $A_{CM} = 0$ and CMRR is improved.

LEVEL SHIFTING STAGE of OPAMP

All the stages are directly coupled to each other. Since the op-amp amplifies the dc signal, stage by stage dc level increases well above ground potential.

Such a high dc level drive the transistor into saturation. It causes distortion in output and limits the maximum voltage swing.

The level shifter brings the dc level down to ground potential when no signal is applied at the input terminals. It is an emitter follower Zi high. It prevents loading of high gain stage.

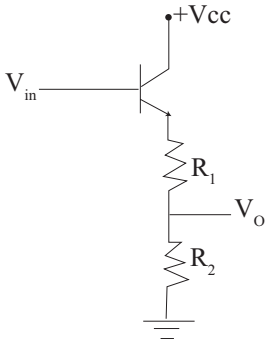


$V_o = V_{in} - V_{BE}$

−ve sign indicates downward shift in level.

$V_{in} - V_{BE} - I(R_1 + R_2) = 0$

$$I = \frac{V_{in} - V_{BE}}{R_1 + R_2}$$



$V_o = IR_2$

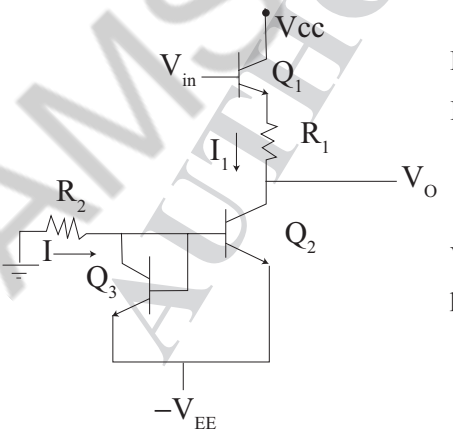
$$V_o = \frac{R_2}{R_1 + R_2}(V_{in} - V_{BE})$$

By proper R_1 & R_2 V_o can be controlled

DRAWBACK:

Signal voltage get accumulated by factor $\frac{R_2}{R_1 + R_2}$

Z_o high

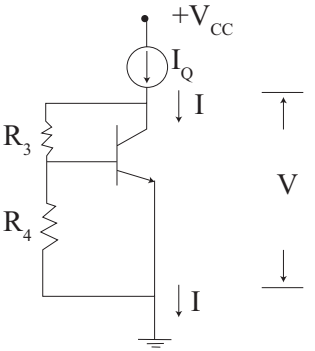


Because of current mirror,

$I_1 = I$

$$I_1 = I = \frac{V_{EE} - V_{BE}}{R_2}$$

$V_o = V_{in} - V_{BE} - I_1R_1$ By proper I & R_1 V_o can be controlled



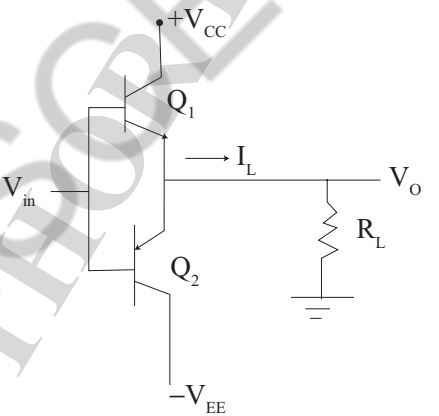
$$V = \frac{V_{BE}}{R_4}(R_3 + R_4) = V_{BE}\left(1 + \frac{R_3}{R_4}\right)$$

It can be used to replace R_1

OUTPUT STAGE of OP-AMP:

Requirements for good output stage are

1. Large output voltage swing
2. Large output current swing
3. Low Output Impedence
4. Low quiescent power dissipation
5. Short circuit protection



When $V_i = +ve$, Q_1 – ON, Q_2 – OFF. Supplies current to load R_L.

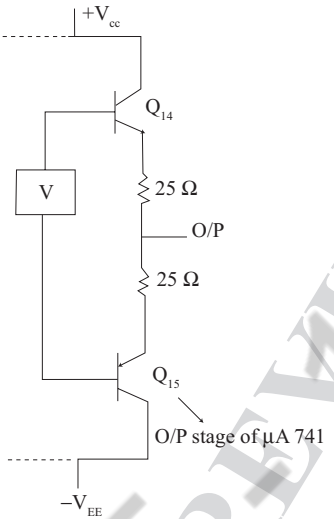
When $V_i = -ve$, Q_1 – OFF, Q_2 – ON, act as sink to remove I from R_L.

But output remains 0 until input exceeds $V_{BE} = 0.5V$.

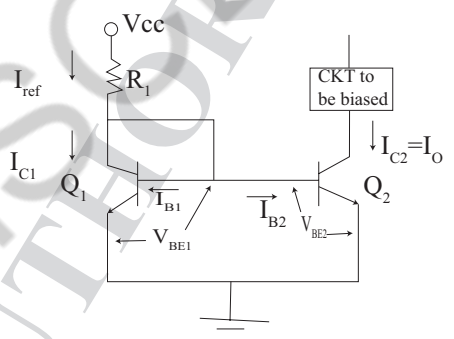
Crossover distortion

It is eliminated by applying bias voltage V greater than $2V_{BE} = 1V$ b/w 2 bases.

Complementary Emitter Follower



2. Explain Constant Current Source (Current Mirror) with necessary circuit and Equations (May 2015)



Base and emitter of Q_1 and Q_2 are tied together So, they have same VBE.

Transistor Q_1 is connected as a diode by shorting its collector to lease.

Since the input current flows through the diode connected transistor, it developer a voltage across the transistor Q_1.

Since Q2 is identical to Q_1, $i_{E2} = i_{E1} = I_{ref}$

As long as Q_2 is maintained in the active region, $i_{E2} = i_{c2} = I_{ref}$

Since the output I is a mirror of I_{ref}, this circuit is referred to as current mirror.

$$I_{c1} = \propto_F I_{ES}\, e^{VBE1/VT}$$

$$I_{c2} = \propto_F I_{ES}\, e^{VBE2/VT}$$

$$\frac{I_{c2}}{I_{c1}} = e^{(V_{BE2} - V_{BE1})/V_T}$$

Since $V_{BE2} = V_{BE}$,

$$I_{c2} = I_{c1} = I_c = I_o$$

$$I_{ref} = I_{c1} + I_{B1} + I_{B2}$$

$$= I_{c1} + \frac{I_{c1}}{\beta_1} + \frac{I_{c2}}{\beta_2}$$

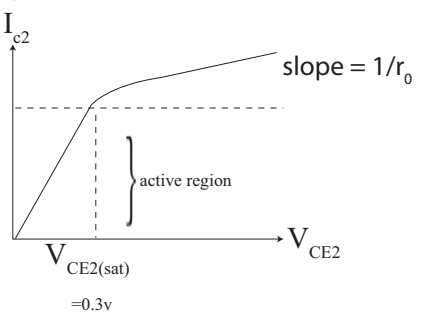
$$I_{ref} = I_{c2}\left(1 + \frac{2}{\beta}\right)$$

$$I_c = I_{ref}\left(\frac{\beta}{\beta + 2}\right)$$

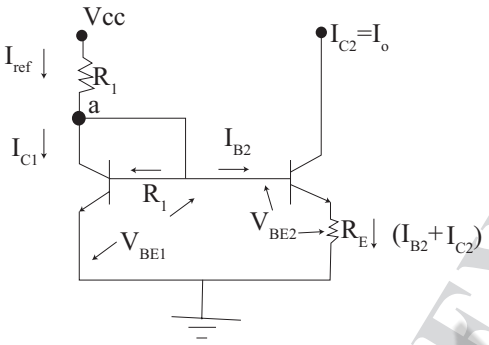
$$I_{ref} = \frac{V_{cc} - V_{BE}}{R_1} \simeq \frac{V_{cc}}{R_1}$$

If $\beta >> 1$

$$I_o = I_c = I_{ref}$$



3. Explain Widlar Current Source & Wilson Current Source



When low value current source is needed wider current source is used

R_E (difference)

$V_{BE2} < V_{BE1}$, $I_o < I_{c1}$

$$\frac{I_{c1}}{I_{c2}} = e^{(V_{BE1}-V_{BE2})/V_T}$$

$$V_{BE2} - V_{BE1} = V_T \text{ in } \left(\frac{I_{c1}}{I_{c2}}\right) \qquad 1$$

Apply KVL to E − B loop

$$V_{BE1} = V_{BE2} + (I_{B2} + I_{c2})R_E$$

$$V_{BE1} - V_{BE2} = \left(\frac{1}{\beta}+1\right) I_{c2} R_E \qquad 2$$

$$\left(\frac{1}{\beta}+1\right) I_{c2} R_E = V_T \text{ in } \left(\frac{I_{C1}}{I_{C2}}\right)$$

$$R_E = \frac{V_T}{\left(\frac{1}{\beta}+1\right) I_{c2}} \text{ in } \left(\frac{I_{C1}}{I_{C2}}\right)$$

At made a,

$V_{ref} = I_{c1} + I_{B1} + I_{B2}$

$$= I_{c1}\left(1+\frac{1}{\beta}\right)+\frac{I_{c2}}{\beta}$$

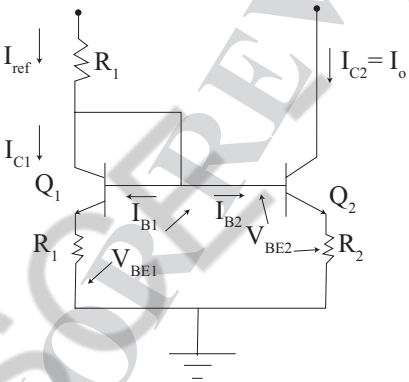
$I_{c2} << I_{c1}$,

$$\therefore \quad I_{ref} = I_{c1}\left(1+\frac{1}{\beta}\right)$$

$$I_{c1} = \frac{\beta}{\beta+1} I_{ref}$$

$$I_{ref} = \frac{V_{cc} - V_{BE}}{R_1}$$

For $\beta >> 1$, $\quad I_{c1} = I_{ref}$



$$V_{BE2} - V_{BE1} = V_T \text{ in } \left(\frac{I_{c2}}{I_{c1}}\right) \qquad 1$$

$$I_{c1}R_1 + V_{BE1} = V_{BE2} + I_{c2}R_2$$

$$V_{BE2} - V_{BE1} = I_{c1}R_1 - I_{c2}R_2 \qquad 2$$

$$I_{c1}R_1 - I_{c2}R_2 = V_T \text{ in } \left(\frac{I_{C2}}{I_{C1}}\right)$$

$$I_{c1}R_1 \left(1 - \frac{I_{C2}}{I_{C1}}\frac{R_2}{R_1}\right) = V_T \text{ in } \left(\frac{I_{C2}}{I_{C1}}\right)$$

$$1-\frac{I_{C2}}{I_{C1}}\frac{R_2}{R_1}=\frac{V_T}{I_{c1}R_1}\ \text{ in }\left(\frac{I_{C2}}{I_{C1}}\right)$$

$$\frac{I_{C2}}{I_{C1}}\frac{R_2}{R_1}=1-\frac{V_T}{I_{c1}R_1}\ \text{ in }\frac{I_{C2}}{I_{C1}}$$

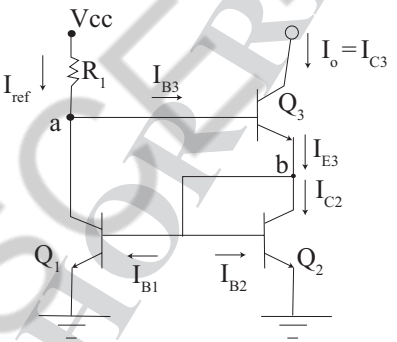
$$\frac{I_{C2}}{I_{C1}}=\frac{R_1}{R_2}=\left(1-\frac{V_T}{I_{c1}R_1}\ \text{ in }\frac{I_{C2}}{I_{C1}}\right)$$

For $0.1 < \frac{I_{c2}}{I_{c1}} < 10$, $\frac{I_{c2}}{I_{c1}} \simeq \frac{R_1}{R_2}$

WILSON CURRENT SOURCE:

In this, output current $I_o = I_{ref}$

Have high output resistance



Since $V_{BE1} = V_{BE2}$,

$$I_{c1} = I_{c2} \quad \& I_{B1} = I_{B2} = I_B$$

At node 'b',

$$I_{E3} = 2I_B + I_{c2}$$

$$I_{E3} = \left(\frac{2}{\beta}+1\right)I_{c2} \qquad 1$$

$$I_{E3} = I_{c3} + I_{B3}$$

$$I_{E3} = I_{c3}\left(1+\frac{1}{\beta}\right) \qquad 2$$

Equate 1 & 2

$$\left(\frac{2}{\beta}+1\right)I_{c2} = I_{c3}\left(1+\frac{1}{\beta}\right)$$

$$I_{c3} = I_o = \left(\frac{\beta+2}{\beta+1}\right)I_{c1} \qquad \text{Since } I_{c2} = I_{c1}$$

At node a,

$$I_{ref} = I_{c1} + I_{B3}$$

$$I_{ref} = \left(\frac{\beta+1}{\beta+2}\right)I_o + \frac{I_o}{\beta}$$

$$= I_o\left(\frac{\beta^2+2\beta+2}{\beta^2+2\beta}\right)$$

$$I_o = \frac{\beta^2+2\beta}{\beta^2+2\beta+2}I_{ref}$$

$$I_{ref} = \frac{V_{cc}-2V_{BE}}{R_1}$$

$$I_o - I_{ref} = \frac{2}{\beta^2+2\beta+2}I_{ref}$$

output resistance is greater = $\beta\frac{r_o}{2}$

4. Explain the INPUT RESISTANCE of OPAMP Internal Circuit

The resistance offered by differential amplifier to the differential input signal $(V_1 - V_2)$ is called differential input resistance R_{id}.

The emitters of Q_1 and Q_2 are floating as R_E is repeated by constant current source.

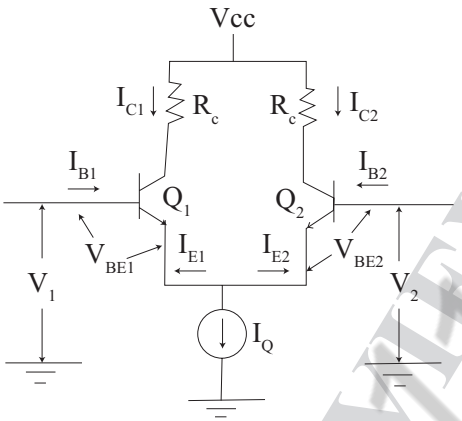
Thus $R_{id} = hie_1 + hie_2 = 2hie$

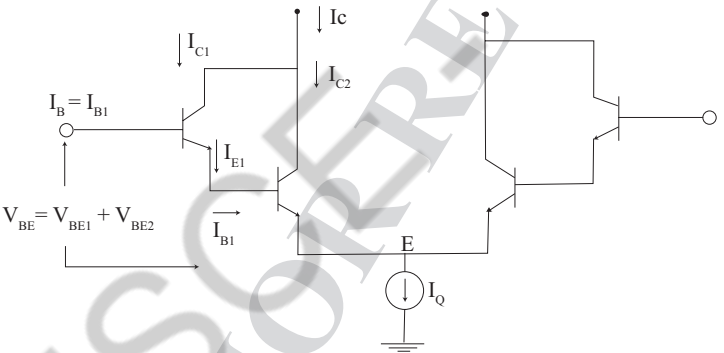
If input 2 is grounded, input 1 is loaded by 2 hie

Hie can be ↑ by ↓ I_B for Q_1 & Q_2

$R = 500\ k\Omega$

Higher value of R can be obtained by using Darlington pair in place of Q_1 & Q_2





For Darlington differential amp, current gain is large

$$\beta = \frac{I_c}{I_{B1}} = \frac{I_{c1} + I_{c1}}{I_{B1}} = \frac{I_{c1}}{I_{B1}} + \frac{I_{c2}}{I_{B1}}$$

$$\beta = \frac{I_{c1}}{I_{B1}} + \frac{I_{c2}}{I_{B2}} \times \frac{I_{B2}}{I_{B1}}$$

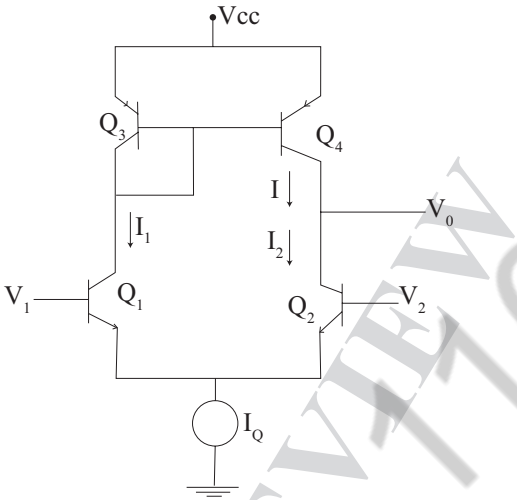
$$\beta = \beta_1 + \beta_2 (\beta_1 + 1)$$

$$\beta = \beta_1 \beta_2$$

If the current gain of each transistor is 100,

Overall current gain = 10,000

5. How Differential Amplifier can be used with Active Load:



For A often circuit voltage gain to be large, gain stages have to be cascaded. But this will ↑ the phase shift.

We can increase the gain by using large R_c. Since gain $\propto R_c$

But there is limitation on the value of R_c.

Large value of R_c requires large chip area.

For large R_c, quiescent drop across it increases. So large power supply required to maintain proper quiescent conditions.

For current mirror, dc Resistance = few KΩ , voltage across it is a function of supply voltage and the current is in mA.

For current mirror, dynamic resistance is very high. So, it can be used as active load.

PNP transistors Q_3 and Q_4 farms current mirror circuit.

Constant current I_Q obtained from current mirror.

$$I_1 = I_2 = \frac{I_Q}{2} \qquad \text{[Base I neglected]}$$

$$I_L = I - I_2 = 0$$

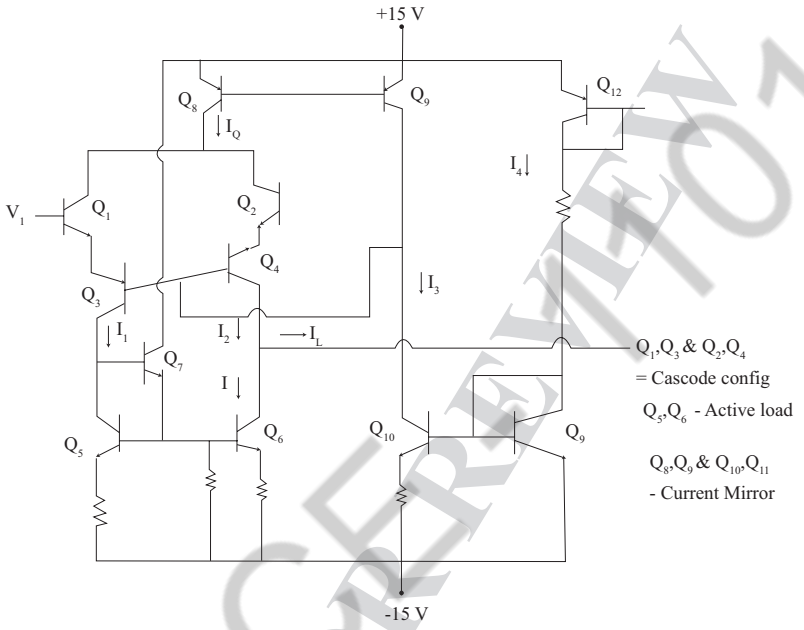
When $V_1 > V_2$, $I_1 \uparrow, I_2 \downarrow$

Since $I_1 + I_2 = I_Q$

Also $I = I_1$

$$I_L = I - I_2 = I_1 - I_2 = g_m V_1 - gmV_2 = gm(V_1 - V_2)$$
$$= gmV_d$$

The circuit thus behave as trans conductance amplifier.



Under quiescent conditions,

$$I_1 = I_2 = \frac{I_Q}{2}$$

$I_L = I_2 - I \qquad I_2 - I_1 = 0$

When $V_1 > V_2$

$I_L = I_2 - I_1$

Thus the circuit behaves as transconductance amp.

6. Discuss about Voltage Reference

It is used to provide constant d.c voltage which act as a reference or standard for other circuits and is independent of parameters like temperature input line voltage, load current etc.

Stability Accuracy Requirement

Temperature co-off of the output voltage of a voltage reference circuit is the measure of the ability of the circuit to maintain the standard output voltage under varying temperature conditions.

$$Tc(V_o) = \frac{\Delta V_o}{\Delta T} \text{ mv/°c} \qquad \text{or} \quad \mu\text{v/°c}$$

$$\% \ Tc(V_o) = 100\left[\frac{\Delta V_o/\Delta T}{V_o}\right]$$

$$= 100\left[\frac{\Delta V_o/V_o}{\Delta T}\right] \qquad \%/°c$$

Voltage ref circuit

1. Constant output V
2. Low output I
3. Stability, accuracy prime considerations

Voltage regulator

1. Constant output V
2. High output I
3. Stability, accuracy are not prime considerations

Performance Parameters Of Voltage Reference Circuits:

Line Regulation:

Effect of change in input line voltage on the output voltage

$$\text{Line regulation} = \frac{\Delta V_o}{\Delta V_i} \text{ mv/v}$$

Load Regulation:

The ability of the circuit to maintain the output voltage under varying load current condition.

$$\text{Line regulation} = \frac{\Delta V_o}{\Delta I_L} \text{ mv/mA}$$

LONG TERM STABILITY:

The ability of the circuit to maintain constant output voltage with respect to time.

Unit = ppm/1000 hrs

RIPPLE RETECTION RATIO:

The input to the reference circuit is usually unregulated. So, output also will get affected by such ripples.

The ability of circuit to reject input ripples and an indication of how much ripples are present at the output due to, input is given by the factor RRR.

$$RRR = 20\log_{10}\left(\frac{V_{ri}}{V_{ro}}\right)$$

V_{ri} = input ripple magnitude

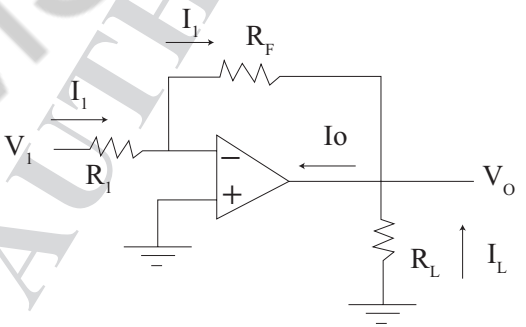
V_{ro} = output ripple magnitude

7. Design an amplifier with a gain of −10 and Ri = 10kΩ

Solution:

$$ACL = \frac{-R_F}{R_I} \quad \Rightarrow \quad -10 = \frac{-R_F}{10}$$

R_F = 100 kΩ



V_i = 1V

R_I = 10 kΩ

R_F = 100 kΩ

$R_L = 25\ k\Omega$

Calculate i) i_1 ii) V_o iii) i_L iv) i_o

Solution:

i) $i_1 = \frac{V_i}{R_1} = \frac{1v}{10k\Omega} = 0.1mA$

ii) $V_o = \frac{-R_F}{R_1} V_i = \frac{-100k\Omega}{10k\Omega}\ 1V = -10V$

iii) $i_L = \frac{V_o}{R_L} = \frac{10v}{25k\Omega} = 0.4mA$

iv) $i_o = i_1 + i_L = 0.1 + 0.4 = 0.5mA$

8. Explain the DC CHARACTERISTICS of Op-AMP:

Ideal op-amp

1. Draws no current from the sow
2. Response independent of temperature

Real op-amp does not work in the same way.

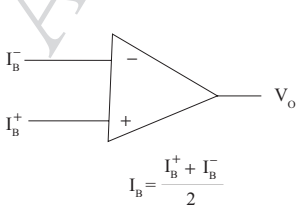
Non-ideal dc characteristics that add error to the output are

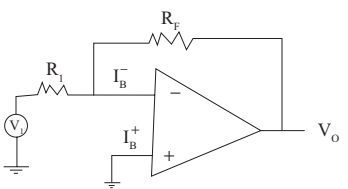
1. Input Bias current
2. Input offset current
3. Input offset voltage
4. Internal drift

(i) Input BIAS CURRENT:

In ideal op-amp. Input terminals does not draw current from the source.

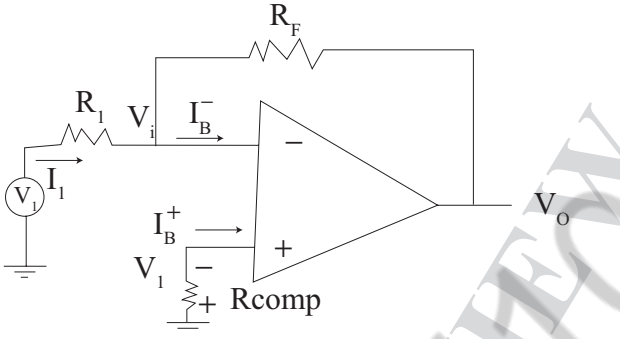
But in practical, it draws some current in order to bias the transistor.





For Bipolar op-amp $I_B = \leq 500$ nA

FET op-amp $I_B = \leq 50$ pA



When $V_i = 0$, $V_o = 0$

But in this $V_o = I_B - R_F$

$$V_o = 500 \text{ nA} \times 1 \text{ mA} = 500 \text{ mV}$$

For compensation, R_{comp} is added.

T_B^+ develops a voltage across R_{comp}

By KVL, $-V_1 + 0 + V_2 - V_o = 0$

$$V_o = V_2 - V_1$$

By choosing proper value of R_{comp}, V_2 can get cancelled with V_1.

$$V_1 = I_B^+ R_{comp}$$

$$I_B^+ = \frac{V_1}{R_{comp}}$$

At node 'a',

$$I_1 = \frac{V_1}{R_1}$$

$I_2 = \dfrac{V_0 + V_1}{R_F}$ for compensation when $V_i = 0$, $V_o = 0$

At node a,

$$I_B^- = I_1 + I_2 = \frac{V_1}{R_1} + \frac{V_1}{R_F} = \frac{V_1(R_1 + R_F)}{R_1 R_F}$$

$$I_B^+ = \frac{V_1}{R_{comp}}$$

Assume $I_B^- = I_B^+$

$$\frac{V_1(R_1 + R_F)}{R_1 R_F} = \frac{V_1}{R_{comp}}$$

$$R_{comp} = \frac{R_1 R_F}{R_1 + R_F} = R_1 \parallel R_F$$

(ii) Input OFFSET CURRENT:

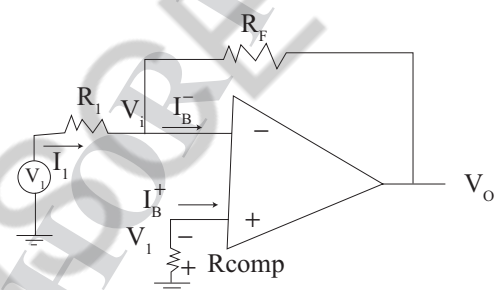
Bias current compensation will work only if $I_B^+ = I_B^-$

But the Input transistors are not identical $I_B^+ \neq I_B^-$

$I_{os} = I_B^+ - I_B^-$

BTT $I_{o3} = 200$ nA

FET $I_{o3} = 10$ pA



$V_1 = I_B^+ R_{comp}$

$$I_1 = \frac{V_1}{R_1}$$

At node 'a',

$I_B^- = I_1 + I_2$

$$I_2 = I_B^- - I_1 = I_B^- - I_B^+ \frac{R_{comp}}{R_1}$$

$$\frac{V_o + V_I}{R_F} = I_2$$

$$V_o = I_2\, Rc - V_I$$

$$V_o = \left(I_B^- - I_B^+ \frac{R_{comp}}{R_I} \right) R_F - I_B^+ R_{comp}$$

Sub the value of R_{comp}

$$V_o = R_F\, [I_B^- - I_B^+]$$

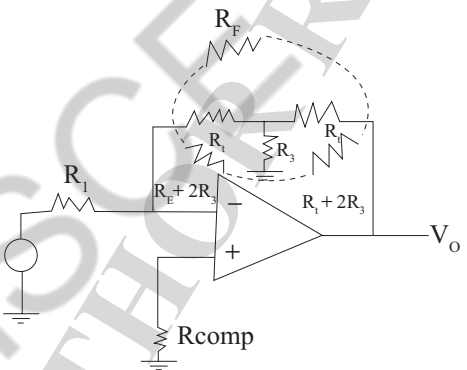
$$V_o = R_F\, I_{os}$$

I_{os} can be minimized by keeping R_F small

For high Z_i, R_I should be large

So, R_F also should be large. Then only we can get high gain.

T – F/B N/W is a good solution.



$$R_F = \frac{R_t^{\,2} + 2R_t R_3}{R_3}$$

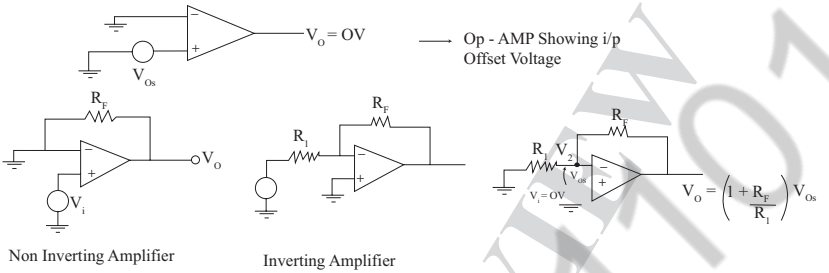
$$R_t << \frac{R_F}{2}$$

$$R_s = \frac{R_t^{\,2}}{R_F - 2R_t}$$

(iii) INPUT OFFSET VOLTAGE:

Even if the compensation techniques are used, $V_o \neq 0$ when $V_i = 0$ due to unavoidable unbalances.

To make the $V_o = 0$, small voltage have to be applied at the input terminals. This is called input offset voltage.



$$V_2 = \left(\frac{R_1}{R_1 + R_F}\right) V_o$$

$$V_o = \left(\frac{R_1 + R_F}{R_1}\right) V_2 - \left(1 + \frac{R_F}{R_1}\right) V_2$$

$$V_{os} = |V_i - V_2| = |-V_2| = V_2$$

$$V_o = \left(1 + \frac{R_F}{R_1}\right) V_{os}$$

TOTAL OUTPUT OFFSET VOLTAGE:

I_B, Vos may be +ve or −ve

So, V_{OT} may be more or less

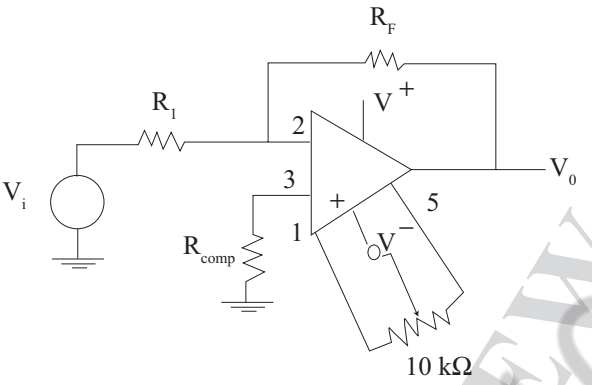
$$V_{oT} = \left(1 + \frac{R_F}{R_1}\right) V_{os} + R_F I_B$$

If R_{comp} is used

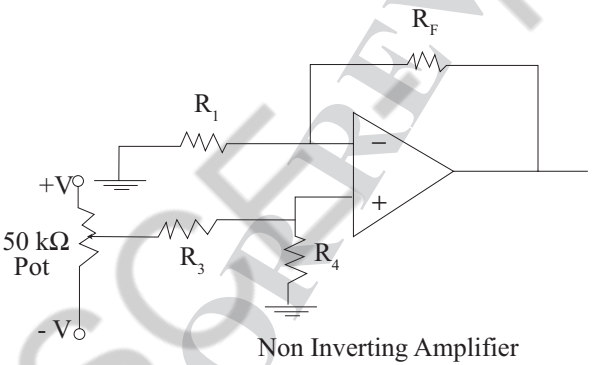
$$V_{oT} = \left(1 + \frac{R_F}{R_1}\right) V_{os} + R_F I_{os}$$

Many op-amps have offset compensation pins to mollify the V_{OT}.

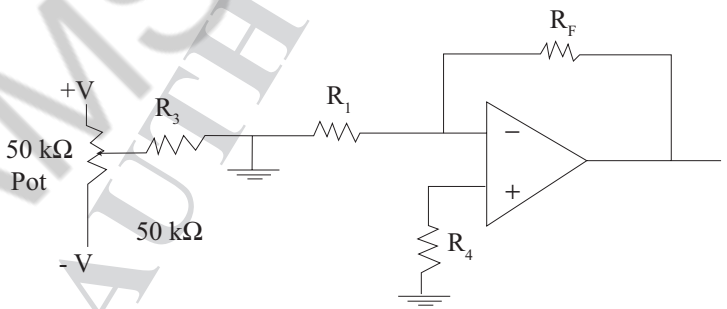
If this pin is not present, balancing circuits are used.



$$V_{os} = \pm \frac{VR_4}{R_3 + R_4}$$



Non Inverting Amplifier



Inverting Amplifier

$$V_{os} = \pm \frac{VR_4}{R_3 + R_4}$$

(iv) THERMAL DRIFT:

I_B, I_{OS}, V_{OS} change with temperature this is called as drift.

I_{OS} drift nA/°c; V_{OS} drift mv/°c

To overcome this.

1. Careful PCB layout
2. Forced air cooling

9. Explain Slew rate and effect of slew rate

SLEW RATE:

Slew rate is defined as maximum rate of change of output with respect to time

Unit = v/μs

$$S.R = S = \left.\frac{dV_o}{dt}\right|_{max}$$

S.R is caused due to

1. Limited changing rate of capacitor
2. Current limiting
3. Saturation of internal stage of op-amp when a high frequency large amplitude signal is applied.

Internal capacitor voltage can't change instantaneously.

$$\frac{dV_c}{dt} = \frac{I}{c}$$

For large charging rate c should be small & I should be high.

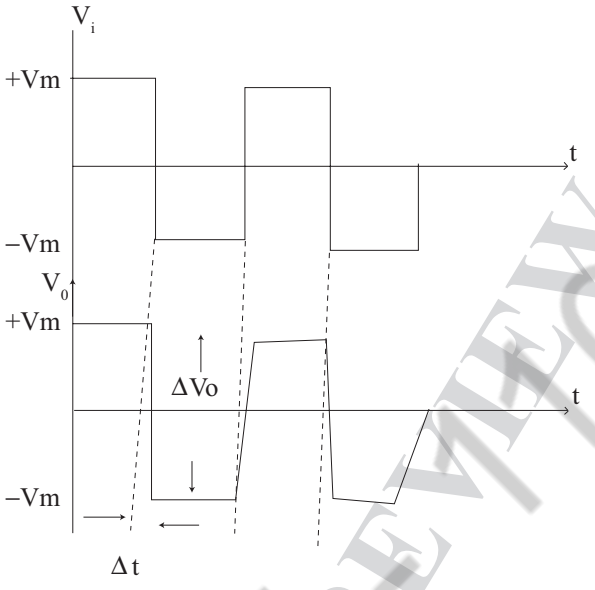
$$\text{Thus} \quad s = \frac{I_{max}}{c}$$

For Ic741, I = 15μA, c = 30PF

$$s = \frac{15\times10^{-6}}{30\times10^{-12}} = \frac{0.5}{10^{-6}} \text{ v/sec}$$

s = 0.5 v/μs

EFFECT OF SLEW RATE:

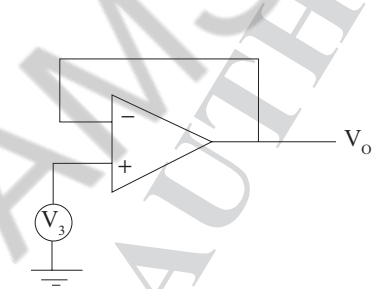


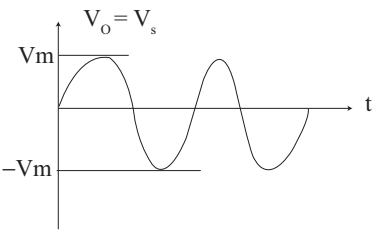
For unity gain op-amp output = input

Here output gets distorted due to S.R.

$$s = \frac{\Delta V_o}{\Delta t} \text{ v/sec}$$

SLEW RATE EQUATION:





Consider voltage follows

$V_s = V_m \sin wt$

$V_o = V_m \sin wt$

$$\frac{dV_o}{dt} = V_m w \cos wt$$

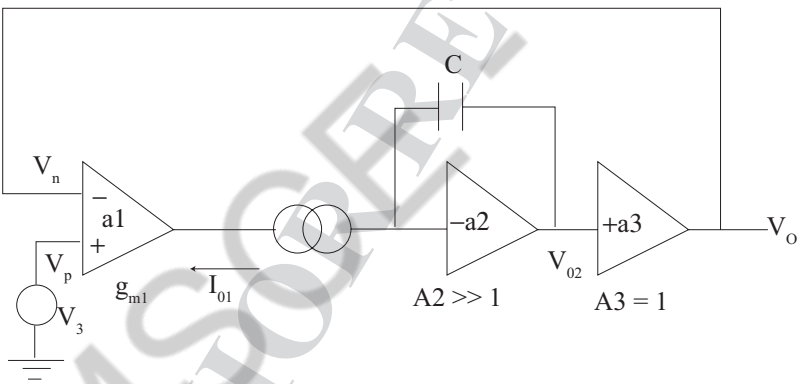
$$S.R = \left.\frac{dV_o}{dt}\right|_{max} = wV_m = 2\pi fV_m \quad V/sec$$

$$S.R = 2\pi fV_m \quad v/sec$$

$$f_{max} = \frac{S.I}{\partial V_m} Hz \qquad \text{full powet B.W}$$

It is the maximum frequency of a large amplitude since wave which op=amp can have without distortion.

10. Explain the Methods Of Improving Slew Rate:



When input overdrives the input stage $I_{max} = \pm I_{o1}(sat)$

Saturation of input stage limits the S.R because under saturation condition, the rate at which capacitor c can charge or discharge is maximum.

$$I_{o1(sat)} = c\frac{dV_{o2}}{dt}$$

$$\frac{dV_{o2}}{dt} = \frac{I_{o1(sat)}}{c}$$

Gain of 3rd stage $a_3 \simeq 1$ Thus $V_o = V_{o2}$

$$\left.\frac{dV_o}{dt}\right|_{max} = \frac{dV_{o2}}{dt} = \frac{I_{o1(sat)}}{c}$$

$$s = \frac{I_{o1(sat)}}{c}$$

Input stage is transconductance amplifier

ie input = V

output = I

For small differential INPUT voltage, relation b/w input voltage & output current is

output current = T_m (differential input)

$$I_{o1} = T_{m1}(V_p - V_n)$$

$$V_{o2} = Z_c T_{m1}(V_p - V_n)$$

$$V_{o2} \simeq V_o \quad \text{as} \quad a_3 \simeq 1$$

$$V_o = Z_c T_{m1}(V_p - V_n)$$

$$= \left[\frac{i}{jwc}\right] Tm_1 \left(V_p - V_n\right)$$

$$Z_c = X_c = \frac{-j}{wc} = \frac{1}{jwc}$$

Op-amp gain = $\dfrac{|V_o|}{|V_p - V_n|}$

$$|a| = \frac{|V_o|}{|V_p - V_n|} = \frac{g_{m1}}{wc} = \frac{g_{m1}}{2\pi fc}$$

$$|a| f = \frac{g_{m1}}{2\pi c}$$

Gain – B.w product = f_t

$$f_t = |a| f$$

$$f_t = \frac{g_{m1}}{2\pi c}$$

$$e = \frac{g_{m1}}{2\pi f_t}$$

$$s = \frac{2\pi I_{o1}(sat)}{g_{m1}} f_t$$

Methods of improving S.R are

1. Increasing f_t:

   Higher f_t, higher S.R.

   $T_o \uparrow f_t$, C have to be $\downarrow$

   Compensating N/w can be used to $\downarrow$ C.

2. Increasing $I_{o1(sat)}$:

   i) This method is difficult

   ii) $T_o \uparrow I_{o1(sat)}$ without affecting f_t and T_{m1}, additional input transistor is designed such that it will go into condition region when large amplitude input signal is applied.

   iii) Such adjustment is possible only in programmable op-amp.

   iv) Separate pin is provided for current setting. Eg) μA 776 by Fairchild, LM346 by National Semiconductor, TL006 by Texas Instrument.

3. REDUCING T_{m1} :

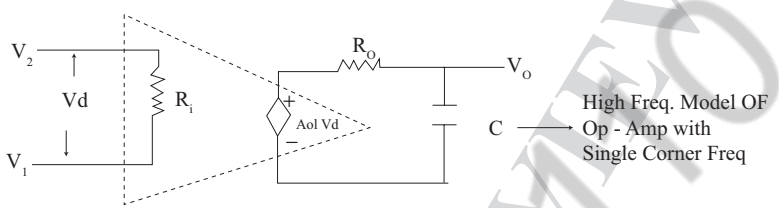
   i) Using resistance in series with emitters of diff. pair

   ii) Using FET instead of BJT diff. pair

11. Explain the FREQUENCY Response of OP-AMP & explain how frequency COMPENSATION is done in Operational Amplifier (May 2015)

Ideal op-amp B.w = ∞ is gain must be constant for all frequencies from 0 to ∞.

But practically, op-amp gain decreases at higher frequencies such a gain reduction with respect to frequency is called roll off.



The dependence of gain of an op-amp on the frequency is because of presence of capacitive component. At higher frequency it offers decreased reactance.

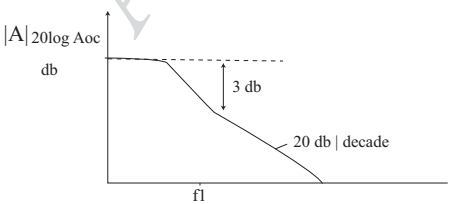
Open loop gain of an op-amp with only one corner frequency,

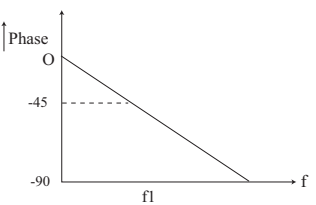
$$Vo = \frac{-jX_c}{R_o - jX_c} A_{oL}\ V_d$$

$$A = \frac{Vo}{V_d} = \frac{A_{oL}}{1 + j2\pi f R_o c} = \frac{A_{oL}}{1 + j\left(f / f_i\right)}$$

$$f_1 = \frac{1}{2\pi R_o c} \quad \text{corner or upper 3dB frequency}$$

$$|A| = \frac{A_{oL}}{\sqrt{1 + \left(f / f_1\right)^2}}; \qquad \phi = -\tan^{-1}\left(f / f_1\right)$$





Voltage transfer function in s-domain

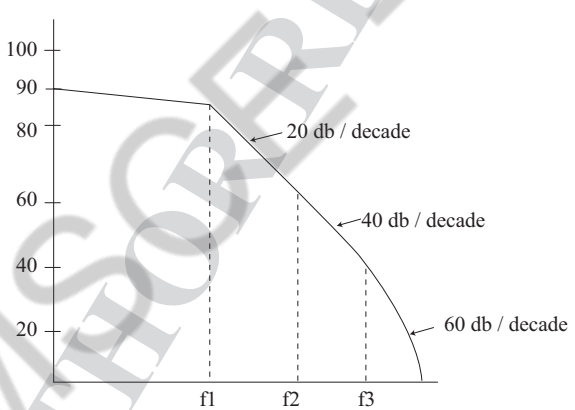
$$A = \frac{A_{oL}}{1 + j\left(\frac{f}{f_i}\right)} = \frac{A_{oL}}{1 + j(w/w_1)} = \frac{A_{oL} w_1}{w_1 + jw}$$

$$= \frac{A_{oL} w_1}{w_1 + s}$$

Practical op-amp has number of stages and each stage produces a capacitive component. Thus due to number of Rc pole pairs, there will be number of different break frequencies.

$$A = \frac{A_{oL}}{\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)} \; ; \; 0 < f_1 < f_2 < f_3$$

$$A = \frac{A_{OL} w_1 \; w_2 \; w_3}{(s + w_1)(s + w_2)(s + w_3)} \; ; \; 0 < w_1 < w_2 < w_3$$



For larger B.w and lower A_{CL}, compensation techniques are used.

i) External Compensation

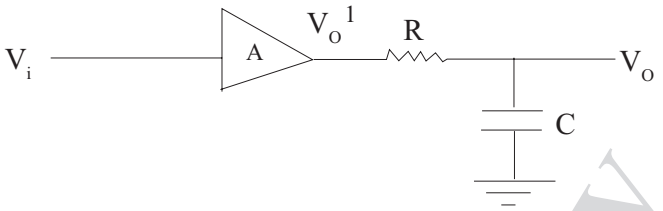
ii) Internal

External Compensation:

i) Dominant Pole Compensation

ii) Pole-Zero (LAG) Compensation

Dominant Pole Compensation:



A = uncompensated T.F in open loop condition.

Introduce a dominant pole by adding R_c N/w

T.F far compensation N/w be A_1

$$A_1 = \frac{V_o}{V_o'} = \frac{-jX_c}{R - jX_c} = \frac{\frac{-j}{wc}}{R - \frac{j}{wc}} = \frac{\frac{-j}{2\pi fc}}{R - \frac{j}{2\pi fc}}$$

$$= \frac{1}{1 + \frac{R}{\left(\frac{-j}{2\pi fc}\right)}} = \frac{1}{1 + j2\pi fRc}$$

$$F_d = \frac{1}{2\pi Rc}$$

$$A_1 = \frac{1}{1 + j\left(f/f_d\right)}$$

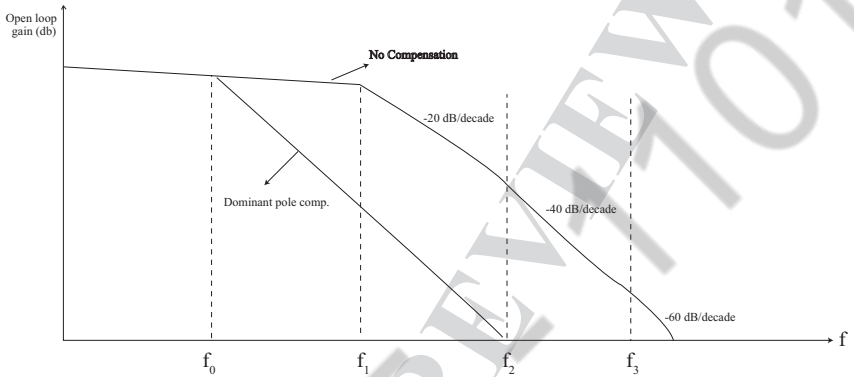
Compensated T.F $A' = A.A_1$

$$A' = \frac{A}{1 + j\left(f/f_d\right)}$$

Where $A = \dfrac{A_{OL}}{\left(1 + j\, f/f_1\right)\left(1 + j\, f/f_2\right)\left(1 + j\, f/f_3\right)}$

Thus $A' = \dfrac{A_{OL}}{\left(1+j\,f/f_d\right)\left(1+j\,f/f_1\right)\left(1+j\,f/f_2\right)\left(1+j\,f/f_3\right)}$; $f_o < f_1 < f_2 < f_3$

The values of k and c are selected in such a way that open loop gain drops to zero with a slope of −20 dB/decade at a frequency where the poles of uncompensated T.F A contribute negligible phase shift.



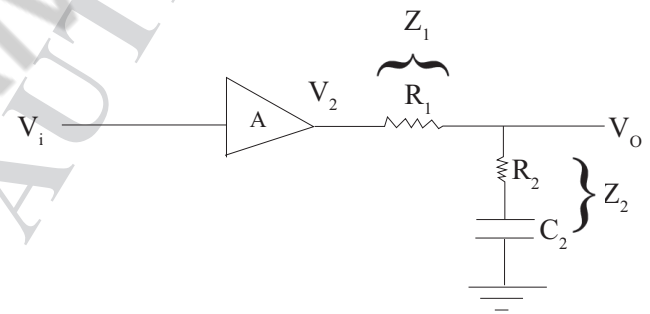
Advantages:

1. Improved noise immunity
2. By adjusting f_d, adequate phase margin and stability of the system is assured.

Disadvantage:

B.W reduce

Pole-Zero Compensation:



$$A_1 = \frac{V_0}{V_2} = \frac{Z_2}{Z_1 + Z_2} = \frac{R_2 - jX_{c2}}{R_1 + R_2 - jX_c} = \frac{R_2 - \frac{j}{wc_2}}{R_1 + R_2 - \frac{j}{wc}}$$

$$= \frac{1 + \frac{R_2}{\left(\frac{-j}{wc}\right)}}{\frac{R_1 + R_2}{\left(-j/wc\right)} + 1}$$

$$= \frac{1 + \frac{R_2}{\left(\frac{-j}{2\pi fc_2}\right)}}{\frac{R_1 + R_2}{\left(-j/2\pi fc_2\right)} + 1} = \frac{1 + j2\pi fR_2c_2}{1 + j(R_1 + R_2)2\pi fc_2}$$

$$A_1 = \frac{1 + j\left(f/f_1\right)}{1 + j\left(f/f_0\right)}$$

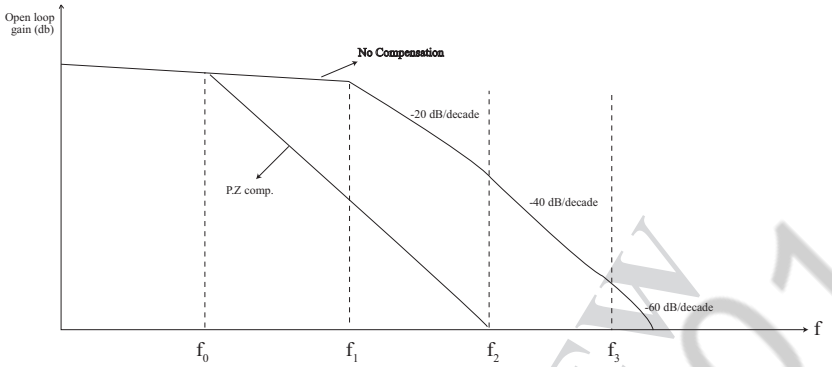
$$f_1 = \frac{1}{2\pi R_2 c_2}$$

$$f_0 = \frac{1}{2\pi(R_1 + R_2)c_2}$$

$$A' = A \cdot A_1$$

$$A' = \frac{A_{OL}\left(1 + j\,f/f_1\right)}{\left(1 + j\,f/f_d\right)\left(1 + j\,f/f_2\right)\left(1 + j\,f/f_3\right)\left(1 + j\,f/f_0\right)}$$

$$A' = \frac{A_{OL}}{\left(1 + j\,f/f_2\right)\left(1 + j\,f/f_3\right)\left(1 + j\,f/f_0\right)}$$

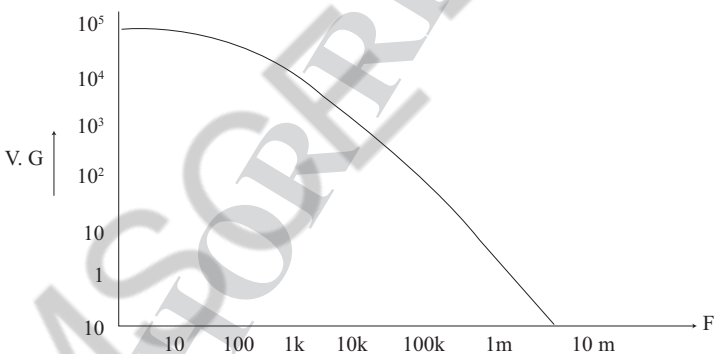


INTERNAL COMPENSATION:

In instrumentation circuit, op-amp have to amplify relatively slow changing signals. Thus it does not need high frequency response.

In this, internally compensated op-amp are used.

They are stable regardless of A_{CL} and without any external components.



Ic 741 has C1 = 30pF, it shanks off signal current thus reduces the output signal at higher frequency.

The internal capacitance is an internal compensating component causes open loop gain to roll off at −20 dB/decade. Thus assures stable circuit.

Ic741, Gain × B.w = 1MHz

Ic741, gain = 10^4 or 80dB, B.w = 1MHz

gain = 10^2 , B.w = 10KHz

gain = 1 , B.w = 1MHz

Eg) Fairchild μA741, National semiconductor LM741, LM101, LM112, Motorola MC1558.

UNIT - 2

APPLICATION OF OPERATIONAL AMPLIFIERS

PART A

1. **Mention some of the linear applications of op-amps. (DEC 09)**
   Adder, subtractor, voltage - to - current converter, current - to - voltage converters, instrumentation amplifier, analog computation, power amplifier, etc are some of the linear op-amp circuits.

2. **Mention some of the non-linear applications of op-amps:**
   Rectifier, peak detector, clipper, clamper, sample and hold circuit, log amplifier, anti-log amplifier, multiplier are some of the non – linear op-amp circuits.

3. **What are the areas of application of non-linear op-amp circuits?**
   1. Industrial instrumentation
   2. Communication
   3. Signal processing

4. **What is voltage follower? (MAY 2010)**
   A circuit in which output folloes the input is called voltage follower.

5. **What is the need for an instrumentation amplifier?**
   In a number of industrial and consumer applications, the measurement of physical quantities is usually done with the help of transducers. The output of transducer has to be amplified So that it can drive the indicator or display system. This function is performed by an instrumentation amplifier.

6. **List the features of instrumentation amplifier:**
   1. High gain accuracy
   2. High CMRR
   3. High gain stability with low temperature co-efficient
   4. Low dc offset
   5. Low output impedance

7. What are the applications of V-I converter?

1. Low voltage dc and ac voltmeter
2. L E D
3. Zener diode tester

8. Define Bandpass filter. (MAY 2010)

The bandpass filter is the combination of high and low pass filters, and this allows a specified range of frequencies to pass through.

9. Write transfer function of op amp as an integer. (MAY 2010)

The transfer function of the integer is

$$|A| = 1/\omega R1cf$$

10. What do you mean by a precision diode?

The major limitation of ordinary diode is that it cannot rectify voltages below the cut-in voltage of the diode. A circuit designed by placing a diode in the feedback loop of an op-amp is called the precision diode and it is capable of rectifying input signals of the order of millivolt.

11. Write down the applications of precision diode.

1. Half - wave rectifier
2. Full - Wave rectifier
3. Peak - value detector
4. Clipper
5. Clamper

12. Define Logarithmic and antilogarithmic amplifier. (MAY 2010)

When a logarithmic PN junction is used in the feedback network of op-amp, the circuit exhibits log or antilog response.

The logarithmic amplifier is a current to voltage converter with the transfer characteristics v0=vi In(If/Ii)

Antilog amplifier is a decoding circuit which converts the logarithmically encoded signal back to the original signal levels as given by $vl = vR10^{-kvi}$

13. Differentiate Schmitt trigger and comparator. (MAY 2010)

S.No	Comparator	Schmitt trigger
1	It compares the input signal with references voltage then yields the output voltage	It operates between two reference points namely UTP&LTP.
2	It need not consist of feedback	It employs positive feedback
3	Comparator output need not to be square wave	Its output is square wave

14. List the applications of Log amplifiers:

1. Analog computation may require functions such as lnx, log x, sin hx etc. These functions can be performed by log amplifiers

2. Log amplifier can perform direct dB display on digital voltmeter and spectrum analyzer

3. Log amplifier can be used to compress the dynamic range of a signal

15. What are the limitations of the basic differentiator circuit?

1. At high frequency, a differentiator may become unstable and break into oscillations

2. The input impedance decreases with increase in frequency , thereby making the circuit sensitive to high frequency noise.

16. Write down the condition for good differentiation

1. For good differentiation, the time period of the input signal must be greater than or equal to $R_f C1$

2. $T \geq R_f C1$ Where, R_f is the feedback resistance

3. C_f is the input capacitance

17. What is a comparator?(MAY 2010)

A comparator is a circuit which compares a signal voltage applied at one input of an op- amp with a known reference voltage at the other input. It is an open loop op - amp with output $\pm$ Vsat .

18. What are the applications of comparator?

1. Zero crossing detector

2. Window detector

3. Time marker generator

4. Phase detector

19. What is a Schmitt trigger? (DEC 09 & MAY 10)

Schmitt trigger is a regenerative comparator. It converts sinusoidal input into a square wave output. The output of Schmitt trigger swings between upper and lower threshold voltages, which are the reference voltages of the input waveform.

20. What is a multivibrator?

Multivibrators are a group of regenerative circuits that are used extensively in timing applications. It is a wave shaping circuit which gives symmetric or asymmetric square output. It has two states either stable or quasi- stable depending on the type of multivibrator.

21. What do you mean by monostable multivibrator?

Monostable multivibrator is one which generates a single pulse of specified duration in response to each external trigger signal. It has only one stable state.

Application of a trigger causes a change to the quasi-stable state.An external trigger signal generated due to charging and discharging of the capacitor produces the transition to the original stable state.

22. What is an astable multivibrator?

Astable multivibrator is a free running oscillator having two quasi-stable states. Thus, there is oscillations between these two states and no external signal are required to produce the change in state.

23. What is a bistable multivibrator?

Bistable multivibrator is one that maintains a given output voltage level unless an external trigger is applied. Application of an external trigger signal causes a change of state, and this output level is maintained indefinitely until an second trigger is applied. Thus, it requires two external triggers before it returns to its initial state

24. Mention any two audio frequency oscillators.

i. RC phase shift oscillator

ii. Wein bridge oscillator

25. What are the characteristics of a comparator?

1. Speed of operation
2. Accuracy
3. Compatibility of the output

26. What is a filter?

Filter is a frequency selective circuit that passes signal of specified band of frequencies and attenuates the signals of frequencies outside the band

27. What are the demerits of passive filters?

Passive filters works well for high frequencies. But at audio frequencies, the inductors become problematic, as they become large, heavy and expensive.For low frequency applications, more number of turns of wire must be used which in turn adds to the series resistance degrading inductor's performance ie, low Q, resulting in high power dissipation.

28. What are the advantages of active filters?

Active filters used op- amp as the active element and resistors and capacitors as passive elements.

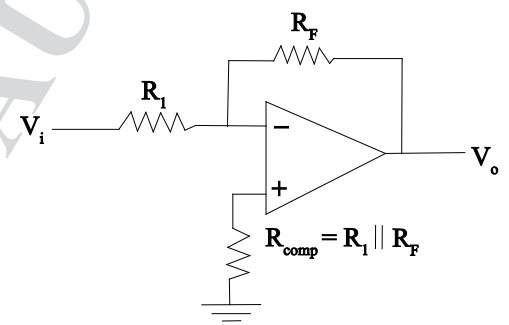
29. Define Low pass filter.

A Low pass filter allows only low frequency signals upto a certain break point fH to pass through.

30. Define High pass filter.

A Low pass filter allows only high frequency signals upto a certain break point fH to pass through

31. Draw the Scale Changer circuit

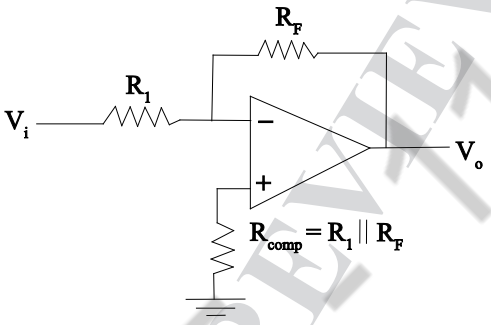


$$\frac{V_o}{V_i} = \frac{-R_F}{R_1} = -k$$

$$V_o = -kV_1$$

Output voltage is k times of input voltage. This is called as scale charger.

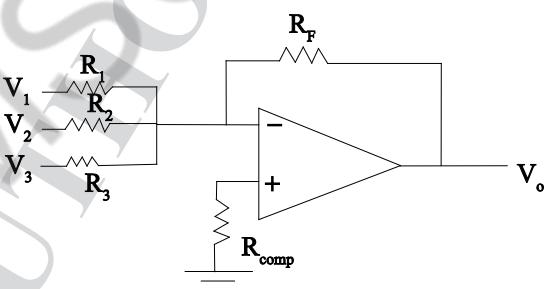
32. Draw the Sign Change/Inverter circuit
Inverter:



$$\text{If } R_F = R_1 \quad V_o = -V_i$$

Output voltage is 180° out of phase with respect to input though the magnitude are same. This is called as inverter.

33. Draw Inverting Summing Amplifier:

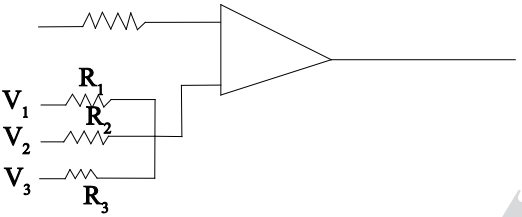


$$V_o = -\left(\frac{R_F}{R_1}V_1 + \frac{R_F}{R_2}V_2 + \frac{R_F}{R_3}V_3\right)$$

$$\text{If} \quad R_1 = R_2 = R_3 = R_F$$

$$V_o = -(V_1 + V_2 + V_3)$$

34. Draw the Non-Inverting Summing Amplifier:



$$V_o = \left(1 + \frac{R_F}{R}\right) V_a$$

$$V_o = \left(1 + \frac{R_F}{R}\right) \frac{\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}}$$

$$\text{If } R_1 = R_2 = R_3 = R = R_F/2$$

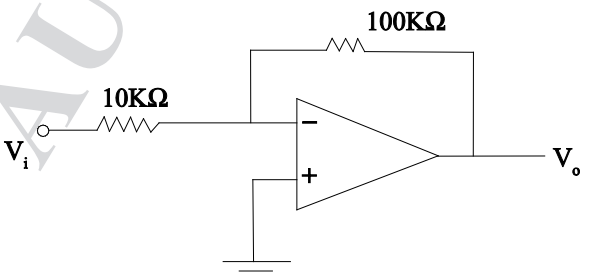
$$V_o = V_1 + V_2 + V_3$$

35. Design an amplifier with a gain of 10 unit resistance equal to 10 kΩ.

$$A_{CL} = \frac{-R_F}{R_1} \qquad \text{Given: } A_{CL} = -10;\ R_1 = 10\ \text{k}\Omega$$

$$-10 = \frac{-R_F}{10\text{k}}$$

$$R_F = 100\ \text{k}\Omega$$

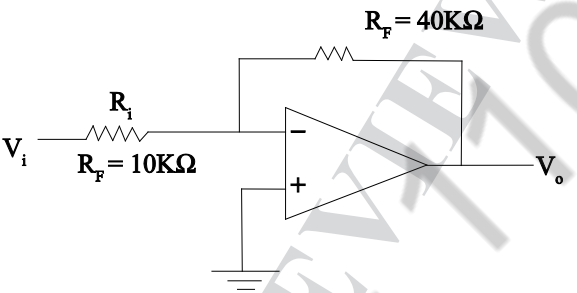


36. Design an amplifier with a gain of +5 using one op-amp.

$$A_{CL} = 1 + \frac{R_F}{R_1} = 5$$

Assume $R_1 = 10\ k\Omega \implies 1 + \frac{R_F}{10k} = 5$

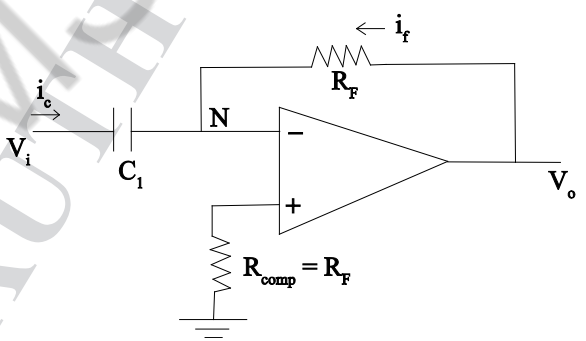
$$\implies R_F = 40\ k\Omega$$



PART-B

1. Explain the OP-AMP Differentiator

In differentiator, the output waveform is the derivative of input waveform.



$$V_o = -R_F C_1 \frac{dV_i}{dt}$$

$$i_c = C_1 \frac{d}{dt}(V_i - V_o) = C_1 \frac{dV_i}{dt}$$

$$i_f = \frac{V_o}{R_F}$$

Nodal eq wrt nodes 'N'

$$C_1 \frac{dV_o}{dt} + \frac{V_o}{R_F} = 0$$

$$V_o = -R_F C_1 \frac{dV_i}{dt}$$

Output voltage V_o is $(-R_F C_1)$times the derivative of input voltage.

$-$ve sign indicates 180° phase shift of output with respect to input.

$$V_o(s) = -R_F C_1 \; s \; V_1(s)$$

$$\frac{V_o(s)}{V_i(s)} = -R_F C_1 \; s$$

Put $s = jw$

$$|A| = \left|\frac{V_o}{V_i}\right| = |-jw \; R_F \; C_1| = wR_F \; C_1$$

$$|A| = \frac{f}{f_a}$$

$$f_a = \frac{1}{2\pi R_F C_1}$$

At f = fa, $|A| = 1$ ie 0dB.

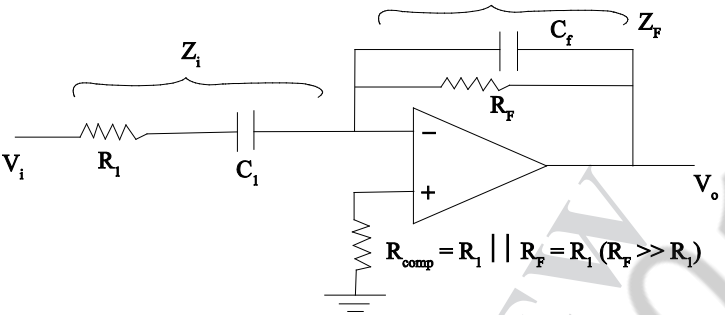
If f ↑ , the gain will ↑ at a rate of 20dB/decade.

At high f, differentiator may become unstable and break into oscillation.

Also, $R_i = \frac{1}{wC_1}$

$R_i \downarrow$ if f ↑ , so the circuit is sensitive to high frequency noise.

Practical Differentiator:



When $R_F\, C_F = R_1\, C_1$

$$\frac{V_o(s)}{V_i(s)} = \frac{-sR_FC_1}{(1+sR_FC_F)(1+sR_1C_1)}$$

$$\frac{V_o(s)}{V_i(s)} = \frac{-sR_FC_1}{(1+sR_1C_1)^2} = \frac{-sR_FC_1}{\left(1+\frac{jf}{f_o}\right)^2}$$

Where $f_b = \dfrac{1}{2\pi R_1C_1}$

When $f < f_b$, gain increases at 20 dB.

When $f > f_b$, gain increases at −20 dB.

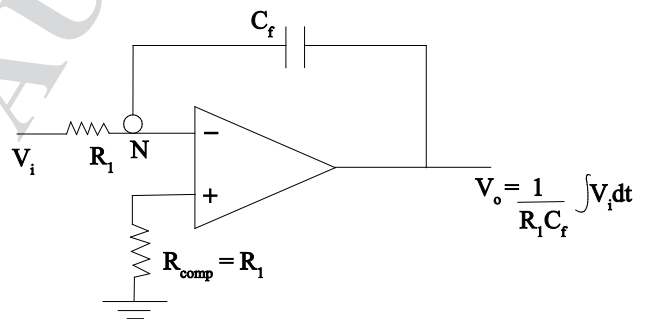
40 dB change in gain is caused by $R_F\, C_F$ & $R_1\, C_1$

Thus the gain at high frequency ↓ thereby avoiding high frequency noise.

$f_a < f_b < f_c$ $\quad f_c$ = unity gain BW

for good differentiation, $T_F \geq R_FC_1$

2. Explain the OP-AMP Integrator circuit



At node N,

$$\frac{V_o}{R_i} + C_f \frac{dV_o}{dt} = 0$$

$$\frac{dV_o}{dt} = -\frac{1}{R_1 C_f} V_i$$

$$\int dV_o = -\frac{1}{R_1 C_f} \int_o^t V_i \, dt$$

$$V_o(t) = -\frac{1}{R_1 C_f} \int_o^t V_i(t) \, dt + V_o(o) \qquad 1$$

$V_o(o)$ = initial output voltage

Thus the output is proportional to the time integral of the input.

$R_1 C_F$ = Time constant

−ve sign indicates that the integrator is a inverting integrator.

$R_{comp} = R_1 \Longrightarrow$ to minimize the effect of input bias current.

For low pass Rc circuit to work as an integrator time constant Rc should be high. It requires large value of R and C. But this is not practically passible.

For Op-amp integrator.

$C_{eq} = C_f(1 - A_v)$

Av = ∞ = Voltage gain. It results in large time constant. It will perform perfect integration.

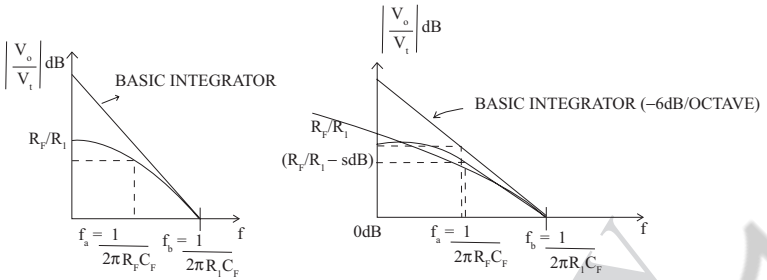
Take L.T for eq 1

$$V_o(s) = -\frac{1}{sR_1 C_f} V_i(s)$$

But s = jw

$$V_o(jw) = -\frac{1}{jwR_1 C_f} V_i(jw)$$

$$|A| = \left|\frac{V_o(jw)}{V_i(jw)}\right| = \left|-\frac{1}{jwR_1 C_f}\right| = \frac{1}{wR_1 C_f}$$



Bode plat is a straight line of slope (−6dB/Octave) or (−20dB/decade).

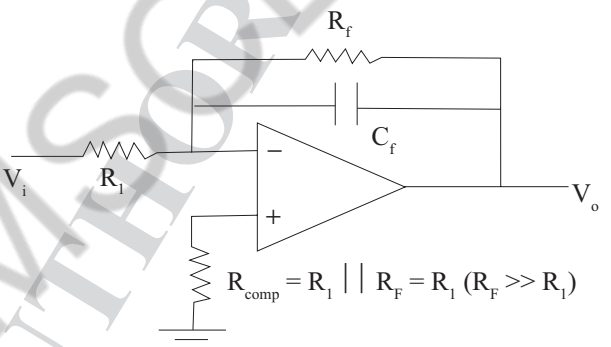
$f_b = \dfrac{1}{2\pi R_1 C_f}$ is the frequency at which gain = 0.

At w = 0, magnitude of transfer function is infinity.

As the gain of the integrator ↓ with ↑ frequency, there is no frequency problem. [Advantage]

But at dc, the gain becomes infinite since the op-amp operate in open loop. [Disadvantage]

Practical Integrator:



If the feedback capacitor is should by a feedback resistor, the gain of an integrator can be limited to avoid saturation problem.

The parallel cancellation of R_f and C_f results in power dissipation.

So, the practical integrator can also be called as easy integrator.

$$\frac{V_i(s)}{R_1} + s\,C_f V_o(s) + \frac{V_o(s)}{R_f} = 0$$

$$V_o(s) = -\frac{1}{sR_fC_f + R_1/R_f} V_i(s)$$

$$|A| = \frac{V_o(jw)}{V_i(jw)} = \frac{1}{\sqrt{w2R_1^2C_f^2 + R_1^2/R_f^2}} = \frac{R_f/R_1}{\sqrt{1+(wR_fC_f)^2}}$$

At w = 0, $|A| = R_f/R_1$

At f = fa, the gain is 0.707 (R_f/R_1) or (−3 dB below R_f/R_1)

$$\sqrt{1+(wR_fC_f)^2} = \sqrt{2}$$

$$fa = \frac{1}{2\pi R_fC_f}$$

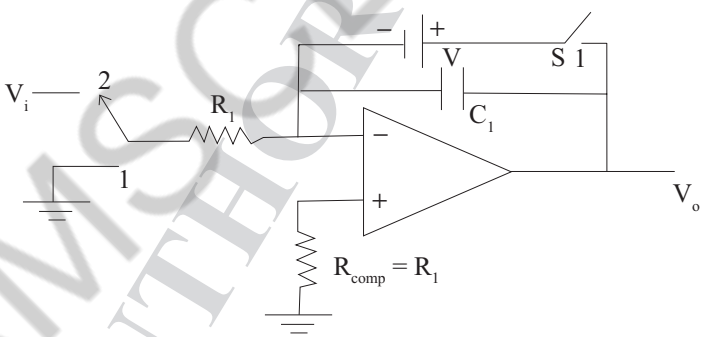
fa specifies where the useful integration starts.

If f < fa ⟹ no integration

If f = fa ⟹ 50% accuracy

If f > 10fa ⟹ 99% accuracy

Integrator With Initial Conditions:



When switch s in position 1, capacitor gets, charged to the voltage V,

Thus $V_o(0) = V$

When switch s in position 2, amplifier is connected as in integrator,

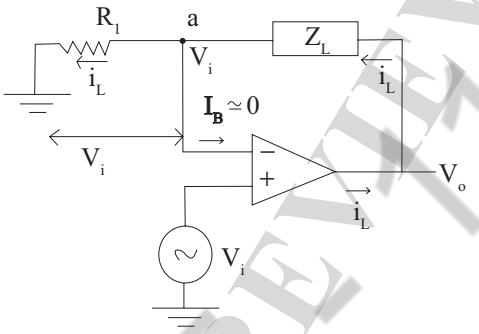
Thus $$V_o(t) = \frac{-1}{R_1C_f}\int_o^t V_i(t)dt + V_o(o)$$

$$V_o(t) = -\frac{1}{R_1 C_f}\int_o^t V_i(t)dt + V$$

3. Explain the Voltage To Current Converter: [Transconductance Amplifier]

V – I converter with floating load.

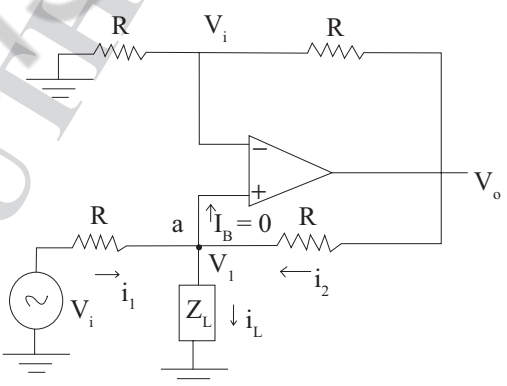
V – I converter with grounded load.



At node a, $V_i = i_L R_1 \implies i_L = \frac{V_i}{R_1}$

ie the output voltage is converted into output current which is equal to V_i/R_1.

Same current flows through the signal source & the load. So, the signal source be capable of providing this load current.



At node a,

$$i_1 + i_2 = i_L$$

$$\frac{V_i - V_1}{R} + \frac{V_o - V_1}{R} = i_L$$

$$V_i + V_o\ 2V_1 = i_L R$$

$$V_1 = \frac{V_i + V_o - i_L R}{2}$$

Since the op-amp is used in non-inverting mode,

$$\frac{V_o}{V_1} = 1 + \frac{R}{R} = 2 \quad \Longrightarrow \quad V_o = 2V_1 = V_i + V_o - i_L R$$

$$V_i = i_L R \quad \Rightarrow i_L = \frac{V_1}{R}$$

Advantages:

Draws very little current from the source, since Z_i of non-inverting amplifier is high.

Applications:

1. Law voltage dc and ac voltmeter.
2. LED
3. Zever diode tester

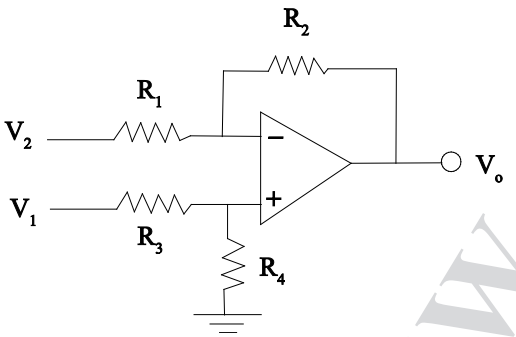
4. Explain Instrumentation Amplifier:

I_A is used to amplify a low level signal in the presence of large common mode component, such as a transducer output in process control & biomedicine.

Features of Instrumentation Amplifier:

- High gain accuracy
- High CMRR
- High gain stability with low temperature co-off
- Low dc offset
- Low output impedance

Consider the basic differential amplifier



$$V_o = -\frac{R_2}{R_1}V_2 + \frac{1}{1+\frac{R_3}{R_4}}V_1\left(1+\frac{R_2}{R_1}\right)$$

$$V_o = -\frac{R_2}{R_1}\left[V_2 - \frac{1}{1+\frac{R_3}{R_4}}\left(\frac{R_1}{R_2}+1\right)V_1\right]$$

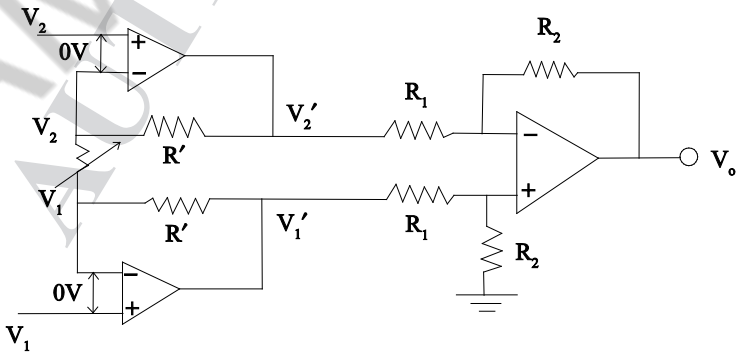
For $R_1/R_2 = R_3/R_4$

$$V_o = \frac{R_2}{R_1}(V_1 - V_2)$$

For source V_1, $Z_i = R_3 + R_4$

V_2, $Z_i = R_1$

This low impendence may load the signal source heavily.



For op-amp A_1 & A_2, $V_d = 0$

When $V_1 = V_2$, voltage across R = 0

As no current flows through R and R′, non-inverting amplifier act as a voltage follower.

Thus $V_2' = V_2$

$V_1' = V_1$

When $V_1 \neq V_2$, current flows in R and R′ and $(V_2' - V_1') > (V_2 - V_1)$

Thus the circuit has differential gain and CMRR compared to the single op-amp circuit.

$$\text{Voltage at this '+' terminal of } A_s = \frac{R_2}{R_1 + R_2} V_1'$$

$$V_0 = \frac{-R_2}{R_1} V_2' + \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_2 V_1'}{R_1 + R_2}\right)$$

$$V_0 = \frac{R_2}{R_1}\left(V_1' - V_2'\right)$$

Since no current flows into op-amp.

$$I = \frac{V_1 = V_2}{R} \quad \text{and passes through } R'$$

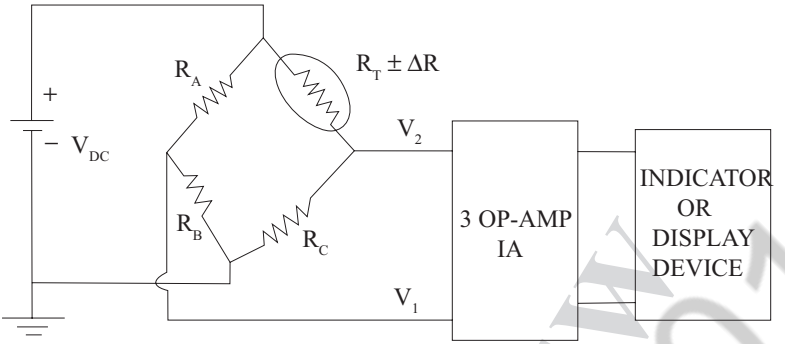
$$V_1' = R'I + V_1 = \frac{R'}{R}\left(V_1 - V_2\right) + V_1$$

$$V_2' = -R'I + V_2 = \frac{-R'}{R}\left(V_1 - V_2\right) + V_2$$

$$\therefore \quad V_0 = \frac{R_2}{R_1}\left[\frac{2R'}{R}\left(V_1 - V_2\right) + \left(V_1 - V_2\right)\right]$$

$$V_0 = \frac{R_2}{R_1}\left(1 + \frac{2R'}{R}\right)\left(V_1 - V_2\right)$$

Diff gain can be varied by 'R'.



In the above figure, R_T changes as a function of physical quantity to be measured.

Initially the bridge is balanced by a dc voltage

Thus $V_1 = V_2$

As the physical quantity changes, R_T will change causing an unbalance in the bridge.

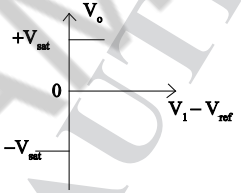
Thus $V_1 \neq V_2$

The differential voltage will be amplified by 3 op-amp I_A.

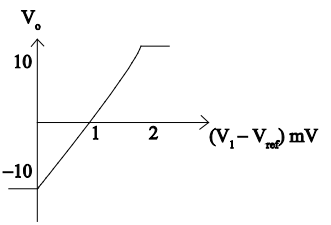
5. Discuss about OP-AMP Comparator:

Comparator compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input.

$V_o = \pm V_{sat}$



IDEAL COMPARATOR

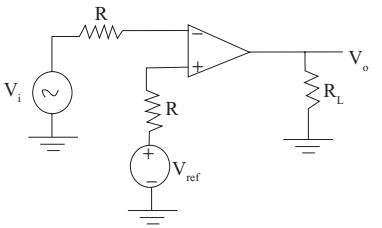


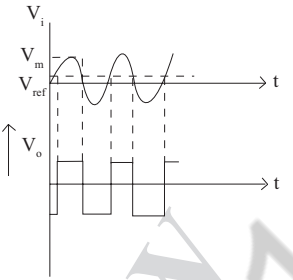
PRACTICAL COMPARATOR

Non-Inverting Comparator:

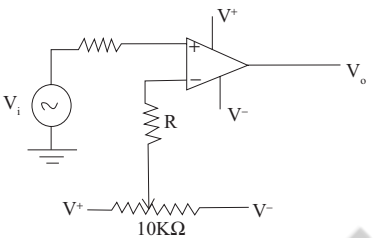
$V_o = -V_{sat}$, $V_i < V_{ref}$

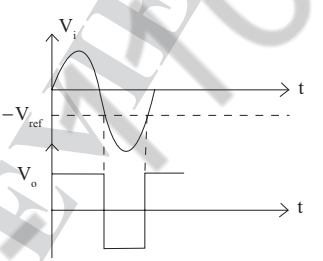
$V_o = +V_{sat}$, $V_i > V_{ref}$





Practical Non Inverting Comparator:

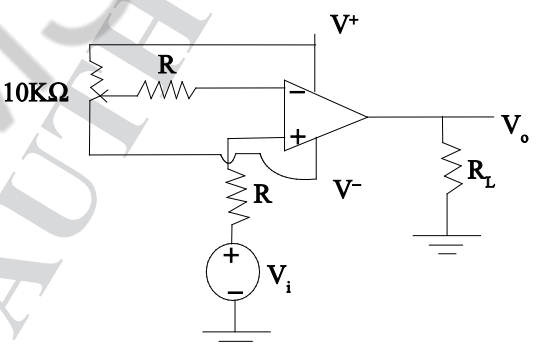




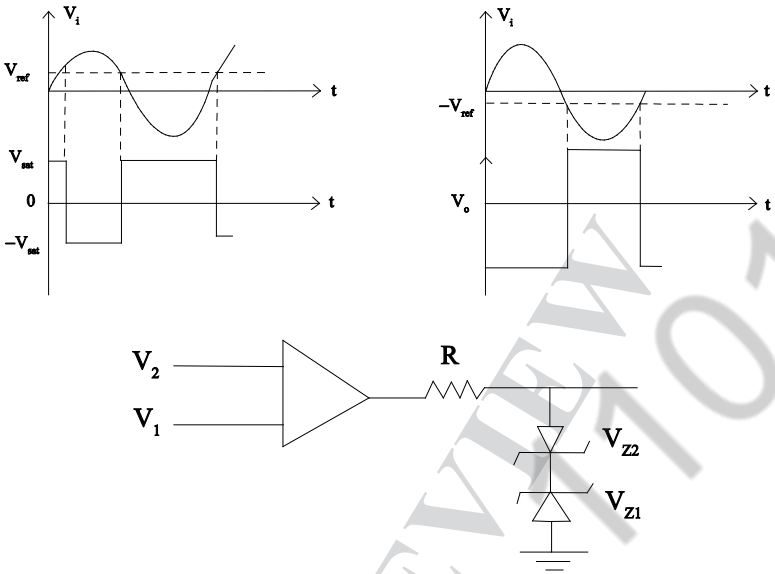
V_{ref} obtained by using 10 kΩ potentiometer which forms a voltage divider with the supply voltage V and V^- with the wiper connected to (−) terminal.

Thus the V_{ref} of desired amplitude and polarity can be obtained.

Inverting Comparator:



$$V_o = V_{sat} \quad , \quad V_i < V_{ref}$$
$$V_o = -V_{sat} \quad , \quad V_i > V_{ref}$$



Comparator using Zener diodes.

Output voltage levels can also be obtained by using Resistor and two back to back Zever diodes.

$$V_o = \pm(V_{Z1} + V_D)$$

$V_D \sim 0.7V$ [Diode forward voltage]

Practically output transistors can't takes place simultaneously. It will take certain amount of time to switch from one level to other.

Thus the waveform will exhibit slanted edges as well as delay at the point of input threshold crossing. This effect is very severe when operating at high frequency.

Thus there is a limit to the operating frequency of a comparator.

For IC 741 (compensated IC),

S.R = 0.5 v/μs

$$t = \frac{2 \times 13}{0.5} = 50\ \mu s \qquad \text{[RESPONSE TIME]}$$

Uncompensated IC makes faster comparators.

For interfacing, the output logic levels should be compatible with logic families (TTL, CMOS, ECL).

To accommodate these needs, monolithic voltage comparators are used.

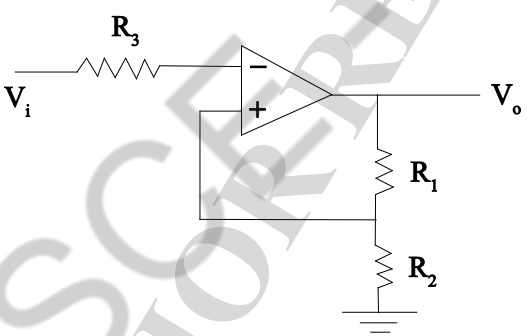
Eg) Fairchild μA 710 & 760 R.T = 40 ns

National LM 111, 160 & 311 R.T = 200 ns

Applications of Comparator:

- Zero crossing detector
- Window detector
- Time market generator
- Phase meter

6. Explain the Regenerative Comparator [Schmit Trigger]:



If positive feedback is added to the comparator, gain can be ↑ , transfer curve becomes class to the ideal one.

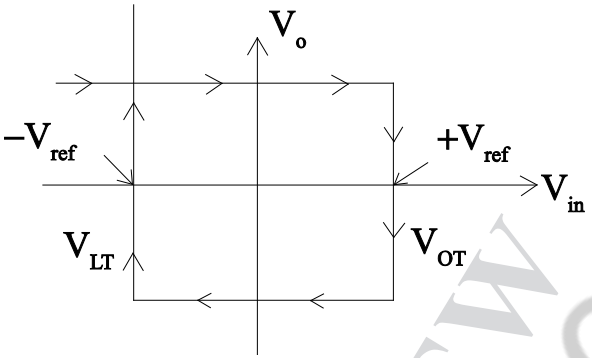
If loop gain $= -B\,A_{OL} = 1$, then $A_{VF} = \infty$

This results in abrupt transition b/w extreme value of Vo. But, practically it is not possible due to supply voltage and temperature variations. So the value greater than unity is chooses.

As the open loop gain is very large, even t small noise can cause triggering to change the output.

The comparator used to avoid such unwanted triggering is called regenerative comparator or Schmit trigger.

This circuit exhibits a phenomenon called hysteresis or backlash.

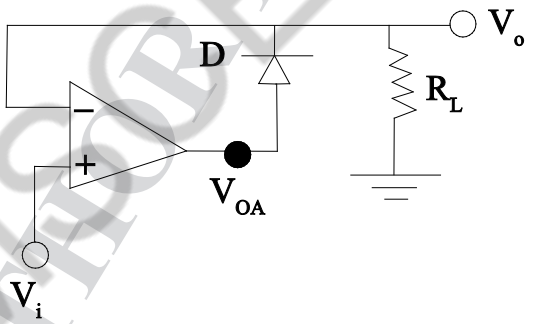


This graph indicates that once the output changes its state, it remains there until input crosses any of threshold voltage level.

This is called dead band or dead zone.

7. Explain Precision Diode Op-Amp Circuits

But in voltage of the ordinary diode is 0.6v. So, it can't rectify voltage below 0.6v. To overcome thus problem, precision diode is used.

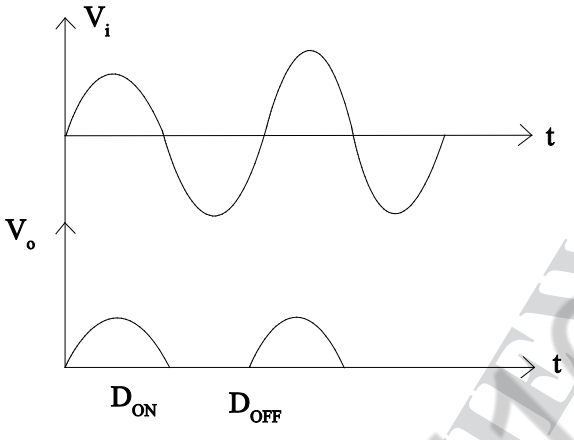


In precision diode, the diode is placed in the feedback loop. Here the cut in voltage V_λ is divided by open loop gain A_{OL}.

When $V_i > V_\lambda / A_{OL}$, output exceeds V_λ and the diode D conducts. Thus the circuit acts like a voltage follower.

Thus $V_o = V_i$

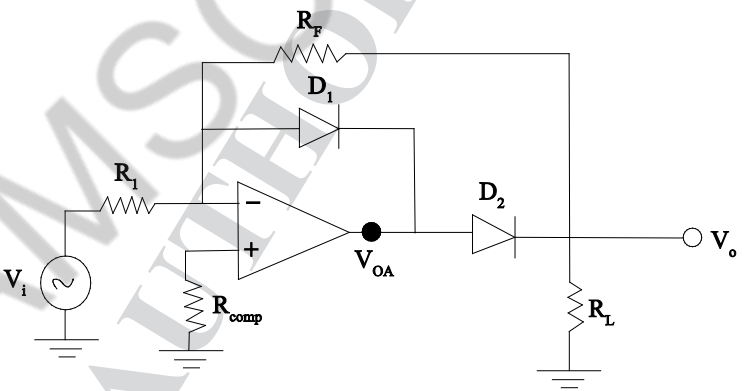
When $V_i < V_\lambda / A_{OL}$, or −ve, diode gets reverse biased. So, no output will be produced.



Applications of Precision Diode:

i. HWR
ii. FWR
iii. Peak Detector
iv. Clipper
v. Clamper

Half Wave Rectifier:



An inverting amplifier can be converted into HWR by adding 2 diodes.

When input is positive,

D_1 = ON D_2 = OFF

Since no current flows through R_F,

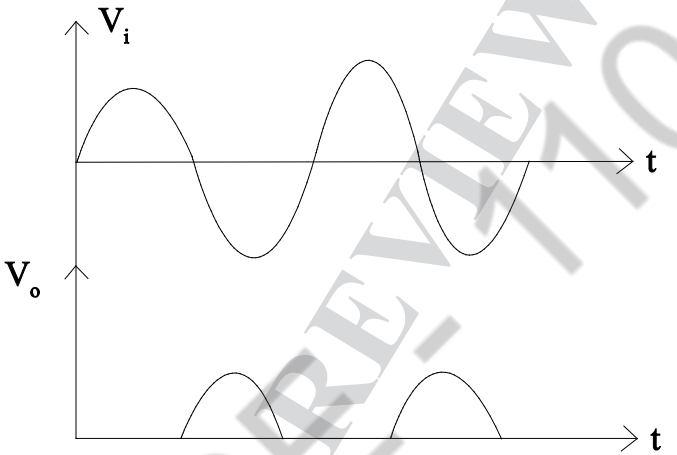
Output Voltage $V_o = 0$

When input is negative,

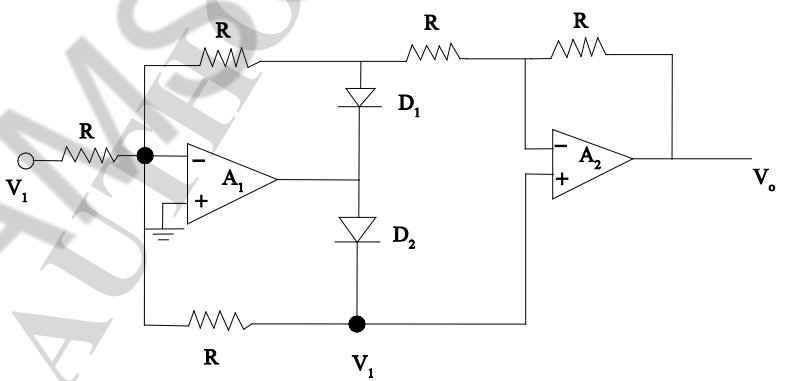
D_1 = OFF D_2 = ON

Thus the circuit will behave as an inverting amplifier when $R_F = R_1$.

$V_o = -V_i$

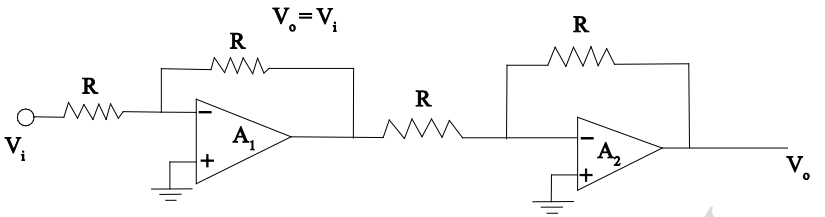


Full Wave Rectifier:



When $V_i > 0$, D_1 = ON ; D_2 = OFF

Thus Both the op-amps will act as inverter.



EQ. CRT FOR $V_i > 0$

When $V_i < 0$, $D_1 = \text{OFF}$; $D_2 = \text{ON}$

Let the output voltage of op-amp A_1 be 'V'.

By applying KCL at node 'a'.

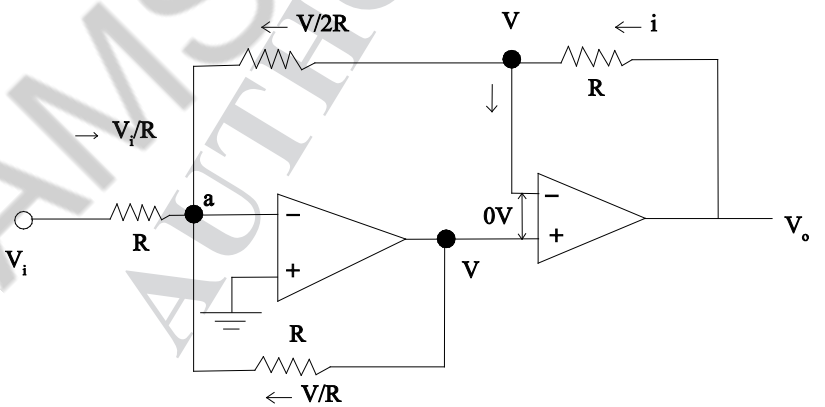
$$\frac{V_i}{R} + \frac{V}{2R} + \frac{V}{R} = 0$$

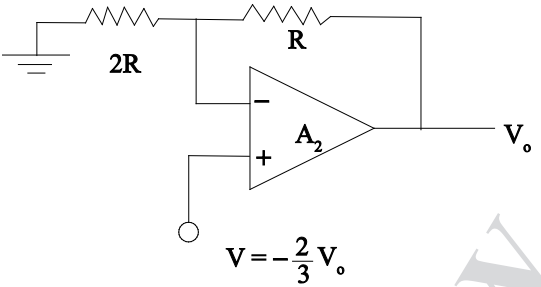
$$V = -\frac{2}{3}V_i$$

The equivalent circuit is a non-inverting amplifier,

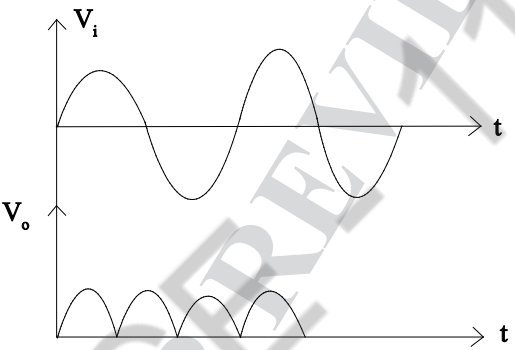
$$V_o = \left(1 + \frac{R}{2R}\right)\left(-\frac{2}{3}V_i\right) = V_i$$

Hence for $V_i < 0$, output is +ve

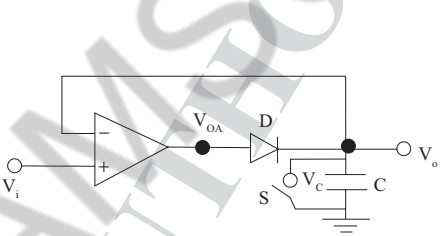


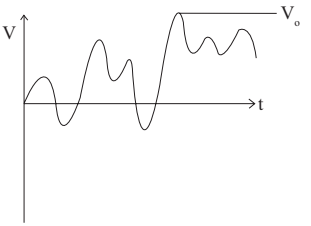


EQ. CRT FOR $V_i = 0$



8. With diagram explain the Peak Detector:





Peak detector is used to compute the peak value of input. It follows the voltage peaks of a signal and stores the highest value on a capacitor.

In peak detector circuit, capacitor output V_c is feed back to the inverting input terminal.

If $V_i > V_c$, output of op-amp will be positive which will forward bias the diode. Thus the circuit will behave as a voltage follower. The never value will be stored in the capacitor.

Thus $V_o = V_1$

If $V_i < V_c$, output of op-amp will be negative which will reverse bias the diode. The capacitor will retain the previous value.

MOSFET switch is used to reset the circuit.

Applications:

1. Testing
2. Measurement instrumentation

9. Explain different OP-AMP Clipper circuit

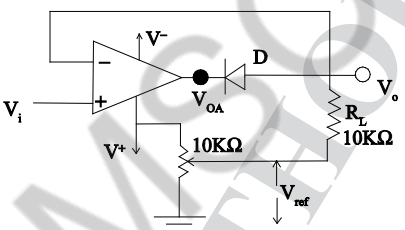
Clipper is used to clip off a certain portion of the input signal to obtain the desired output waveform.

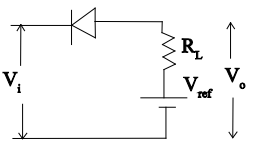
i) Positive clipper

ii) Negative clipper

i) Positive Clipper:

Clipping level is determined by V_{ref} and could be obtained from positive supply voltage V^+.



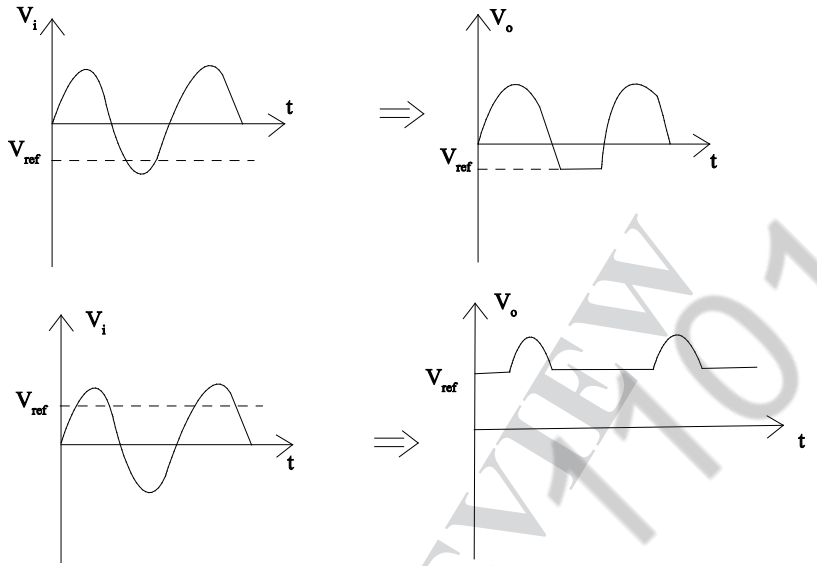


If $V_i > V_{ref}$ or +ve, op-amp output is +ve which will reverse bias the diode. Thus the circuit will operate in open loop,

$$\text{Thus } V_o = V_{ref}$$

If $V_i < V_{ref}$ or −ve, op-amp output is −ve which will forward bias the diode. Thus the circuit will act as voltage follower,

$$\text{Thus } V_o = V_i$$



Negative Clipper:

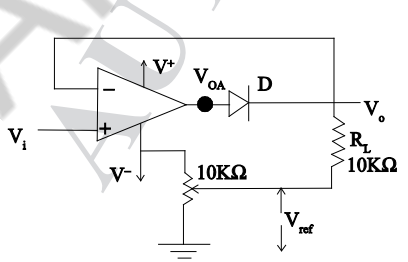
Negative clipper can be formed by just reversing the diode. It will clip off the negative part of the input signal below V_{ref}.

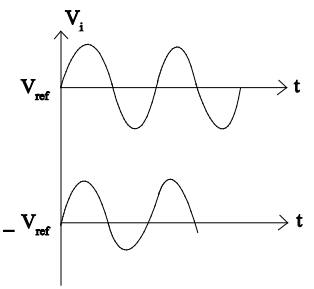
If $V_i > V_{ref}$ or +ve, op-amp output is +ve which will forward bias the diode. Thus the circuit will act as voltage follower,

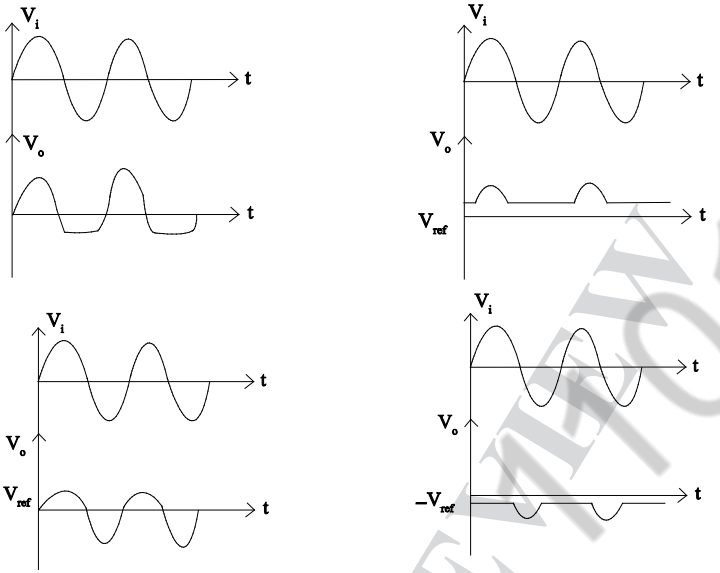
$$V_o = V_i$$

If $V_i < V_{ref}$ or −ve, op-amp output is −ve which will reverse bias the diode. Thus the circuit will operate in open loop made,

$$V_o = -V_{ref}$$







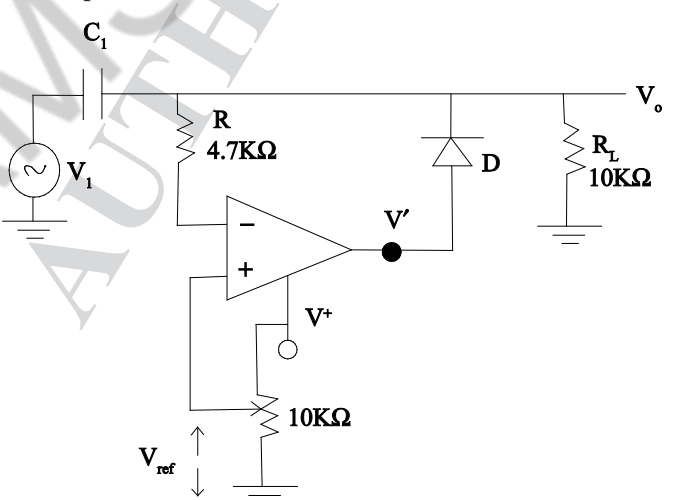
10. Describe briefly about clampers.

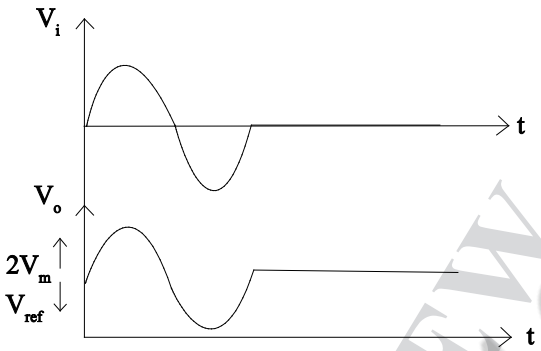
or

DC Inserter or Restorer of Peak Clamper

Clamper is used to add a desired dc level to the output voltage. If the clamped d.c level is positive, it is called as positive clamper. If the clamped d.c level is negative, it is called as negative clamper.

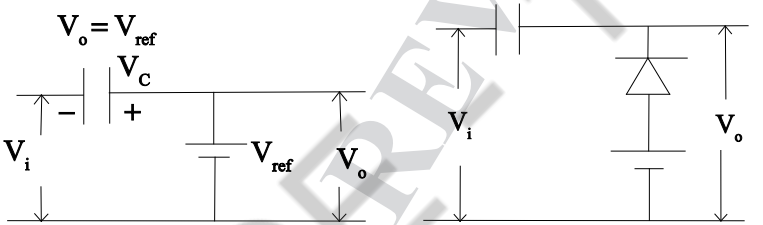
Positive Clamper:





During −ve half cycle of input, diode is forward biased.

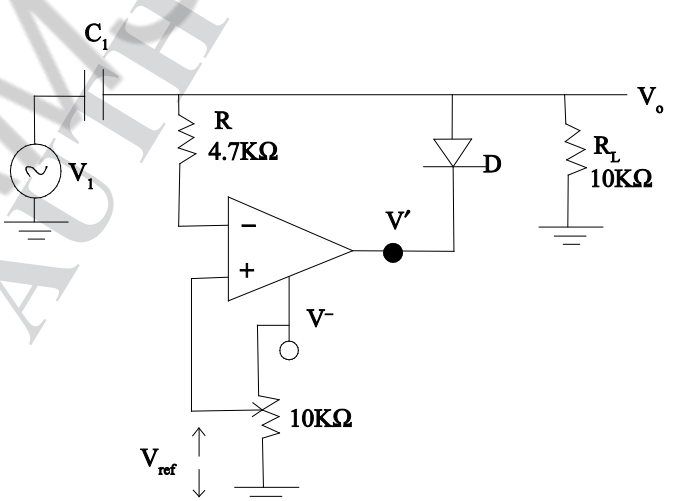
Capacitor charge to V volts

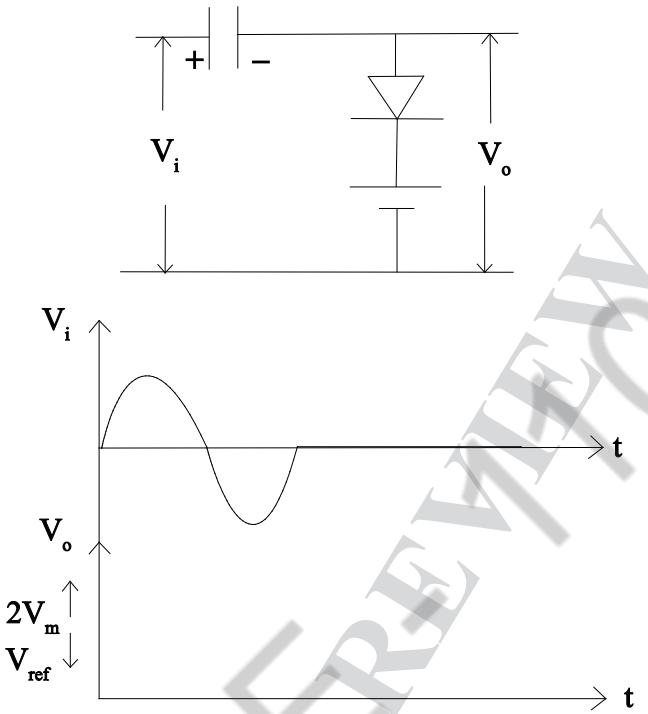


During +ve half cycle, diode reverse biased.

$V_o = V_c - V_i + V_{ref} + V_m$

Negative Clamper:





Negative peak clamper can be obtained by reversing the diode & using $-V_{ref}$.

During +ve

$V_o = -V_{ref}$

During −ve

$V_o = -V_c - V_1 + V_m + V_{ref}$

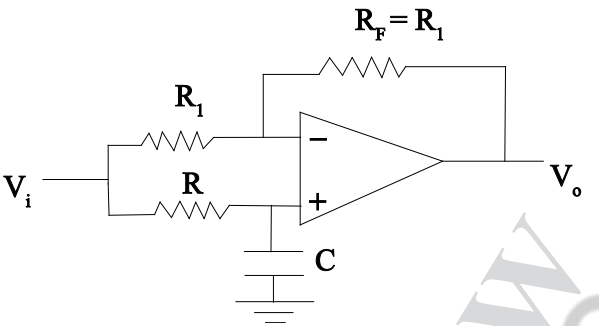
11. Explain different Phase Shift Circuits:

The phase shift circuits produce phase shift or between −180° and +180° and maintain a constant gain.

It is also called as constant delay filters or all pass filters.

Phase Lag Circuits:

Input voltage V_1 drives a simple inverting amplifier with inverting input applied at −ve terminal of op-amp and a non-inverting amplifier with a LPF.



$$V_o(jw) = -V_i(jw) + 2\frac{1}{1+jwRc}V_i(jw)$$

$$\frac{V_o(jw)}{V_i(jw)} = \left(\frac{1-jwRc}{1+jwRc}\right)$$

$$\theta = -\tan^{-1}(wRc) - \tan^{-1}(wRc)$$

$$\theta = -2\tan^{-1}(wRc)$$

$$\theta = -2\tan^{-1}(2\pi fRc)$$

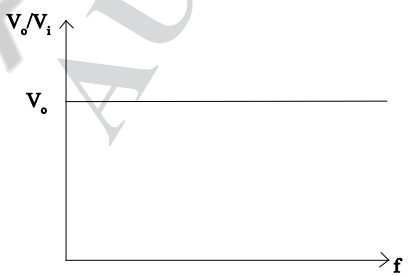
$$\theta = -2\tan^{-1}\left(f/f_o\right)$$

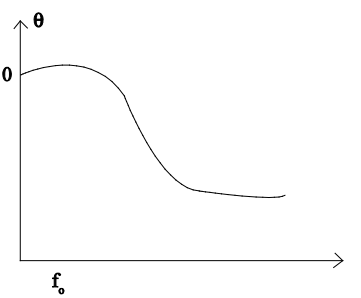
$$f_o = \frac{1}{2\pi Rc}$$

For $w = 0 \implies \theta = 0$

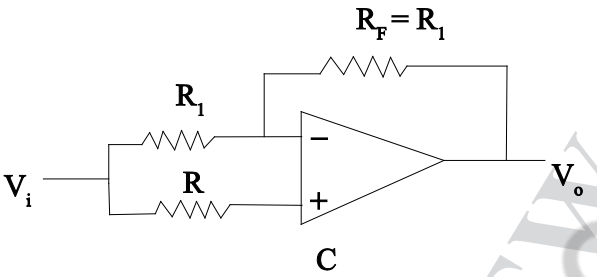
$w = \infty \implies \theta = -180°$

For $f = fo \implies \theta = -90°$





Phase Lead Circuit:



$$V_o(jw) + 2\left(\frac{jwRc}{1+jwRc}\right)V_i(jw)$$

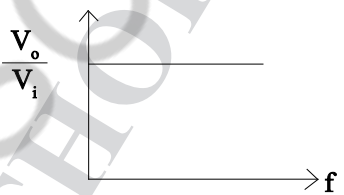
$$\frac{V_o(jw)}{V_i(jw)} = \frac{-1+jwRc}{1+jwRc}$$

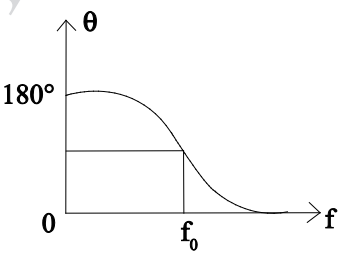
$\theta = 180° - \tan^{-1}(wRc) - \tan^{-1}(wRc)$

$\theta = 180° - 2\tan^{-1}(wRc)$

$\theta = 180° - 2\tan^{-1}(2\pi fRc)$

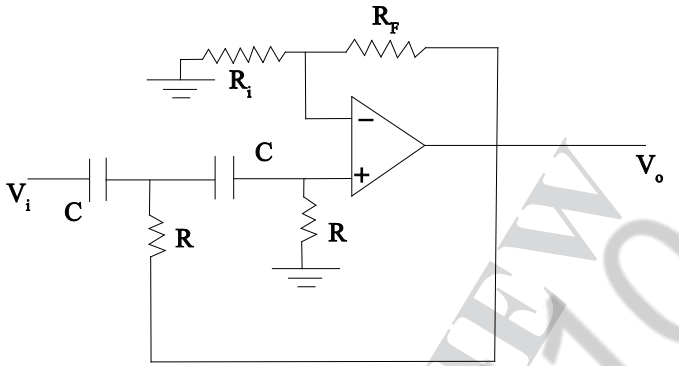
$\theta = 180° - 2\tan^{-1}(f/fo)$





$$f_0 = \frac{1}{2\pi Rc}$$

11. Explain OP-AMP Low pass & High Pass Filter:



Put $y_1 = y_2 = sc$ & $1/3 = 1/4 = G = \frac{1}{R}$

$$H(s) = \frac{A_o s^2}{s^2 + (3 - A_o) w_1 s + w_e^2} \qquad w_e = \frac{1}{Rc}$$

$$H(s) = \frac{A_o}{1 + \frac{w_e}{s}(3 - A_o) + \left(\frac{w_e}{s}\right)^2}$$

For $w = 0$, $H = 0$

$w = \infty$ $H = A_o$

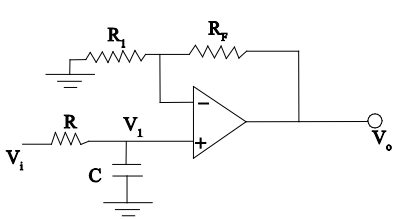
$$f_e = f_{3dB} = \frac{1}{2\pi Rc}$$

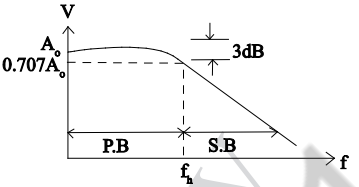
Put $s = jw$ and $3 - A_o = \infty = 1.414$

$$|H(jw)| = \left|\frac{V_o}{V_1}\right| = \frac{A_o}{\sqrt{1 + \left(F_L/f\right)}} \Rightarrow \left|\frac{H(jw)}{A_o}\right| = \frac{1}{\sqrt{1 + \left(F_L/f\right)^4}}$$

For n^{th} order filter $\left|\frac{H(jw)}{A_o}\right| = \frac{1}{\sqrt{1 + \left(F_L/f\right)^n}}$

First Order LPF:





Single R_c N/w connected to '+' terminal.

R_i, R_F determines the gain of filter.

Voltage across capacitor c in s-domain.

$$V_1(s) = \frac{\frac{1}{sc}}{R + \frac{1}{sc}} V_i(s)$$

$$\frac{V_1(s)}{V_i(s)} = \frac{\frac{1}{sc}}{R + \frac{1}{sc}} \Rightarrow \frac{V_1(s)}{V_i(s)} = \frac{1}{Rcs + 1}$$

Based loop gain A_o,

$$A_o = \frac{V_o(s)}{V_1(s)} = 1 + \frac{R_F}{R_i}$$

$$H(s) = \frac{V_o(s)}{V_1(s)} = \frac{V_o(s)}{V_1(s)} \times \frac{V_1(s)}{V_1(s)} = \left(1 + \frac{R_F}{R_i}\right)\left(\frac{1}{Rcs+1}\right)$$

$$= \frac{A_o}{Rcs + 1}$$

Let $$w_h = \frac{1}{Rc}$$

$$H(s) = \frac{A_o}{\frac{s}{w_h} + 1} = \frac{A_o w_h}{s + w_h}$$

$$f_h = \frac{1}{2\pi Rc} \quad \& \quad f = \frac{w}{2\pi}$$

When $f << f_h$

$$|H(jw)| = A_o$$

When $f = f_h$

$$|H(jw)| = A_o/\sqrt{2} = 0.707A_o$$

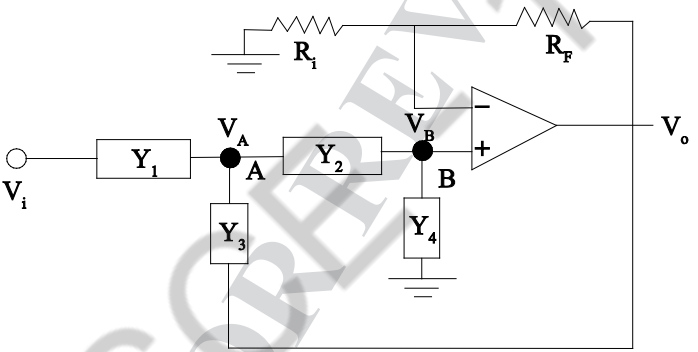
When $f >> f_h$

$$|H(jw)| << A_o \simeq 0$$

Second Order LPF:

Two RC pairs

Roll off = −40 dB/decode



q

$$A_o = 1 + \frac{R_F}{R_i} \Rightarrow \frac{V_o}{V_B} = 1 + \frac{R_F}{R_1} \Rightarrow V_o = V_B\left(1 + \frac{R_F}{R_1}\right) = A_o V_B$$

Apply KCL at node A,

$$(V_A - V_i)Y_1 + (V_A - V_o)Y_3 + (V_A - V_B)Y_2 = 0$$

$$V_i Y_1 = V_A(Y_1 + Y_2 + Y_3) - V_o Y_3 - V_B Y_2$$

$$V_i Y_1 = V_A(Y_1 + Y_2 + Y_3) - V_o Y_3 - \frac{V_o}{A_o} Y_2 \qquad 1$$

Apply KCL at node B,

$$V_A Y_4 + (V_B - V_A)Y_2 = 0$$

$$V_B Y_2 = V_B (Y_2 + Y_4) = \frac{V_o (Y_2 + Y_4)}{A_o}$$

$$V_A = \frac{V_o (Y_2 + Y_4)}{A_o Y_2} \qquad 2$$

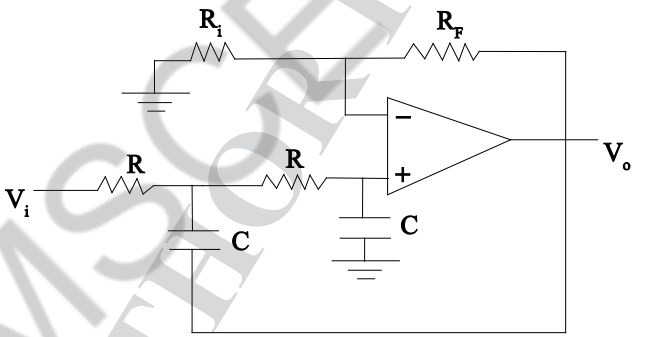
Sub 2 in 1

$$V_i Y_1 = \frac{V_o (Y_2 + Y_4)(Y_1 + Y_2 + Y_3)}{A_o Y_2} - V_o Y_3 - \frac{V_o}{A_o} Y_2$$

$$V_i Y_1 = V_o \left[\frac{(Y_2 + Y_4)(Y_1 + Y_2 + Y_3)}{A_o Y_2} - Y_3 - \frac{Y_2}{A_o} \right]$$

$$\frac{V_o}{V_1} = \frac{A_o Y_1 Y_2}{Y_1 Y_2 + Y_4 (Y_1 + Y_2 + Y_3) + Y_2 Y_3 (1 - A_o)}$$

To make a LPF choose $Y_1 = Y_2 = \frac{1}{R}$ & $Y_3 Y_4 = sc$



$$H(s) = \frac{Ao}{S^2 C^2 R^2 + SCR(3 - Ao) + 1} \qquad 3$$

$H(o) = A_o$; $H\infty = 0$

Minimum dc offset $\frac{R_i R_F}{R_i + R_F} = R + R = ZR$ should be satisfied.

T.R of 2nd order LPF can also be written as

$$H(s) = \frac{A_o w_n^{\ 2}}{s^2 + d w_n s + w_n^{\ 2}} \qquad 4$$

Compare 3 & 4

$$w_n = \frac{1}{Rc} \quad \text{Upper cut off frequency}$$

$\propto = (3 - A_o)$ damping co-off

In 4 but s = jw

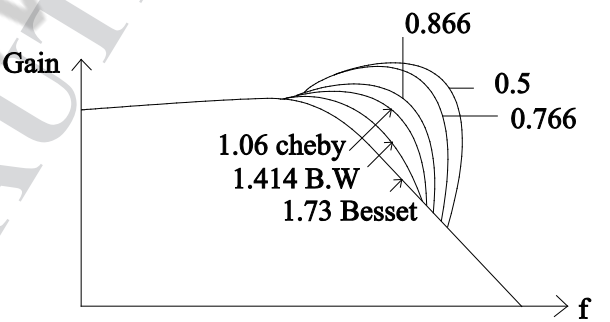
$$H(jw) = \frac{Ao}{\left(\frac{jw}{w_n}\right)^2 + j\alpha\left(w/w_n\right) + 1}$$

$$H(jw) = \frac{Ao}{s^2 + \alpha s + 1}$$

$$s_n = j\left(\frac{w}{w_n}\right) \quad \text{Normalized frequency}$$

$$20\log\left|H(jw)\right| = 20\log\left|\frac{Ao}{1 + j\alpha\left(w/w_n\right) + \left(\frac{jw}{w_n}\right)^2}\right|$$

$$= 20\log\left|\frac{Ao}{\sqrt{\left(1 - \frac{w^2}{w_n^2}\right)^2 + \left(\alpha\frac{w}{w_n}\right)^2}}\right|$$



For $\propto > 1.7$ is heavily damped filter, response is stable.

For B.w filter, $\propto = 1.7$

$$20\log\left|H(jw)\right| = 20\log\left|\frac{V_o}{V_i}\right| = 20\log\frac{A_o}{\sqrt{1+\left(\frac{w}{w_n}\right)^{-4}}}$$

For n[th] order L.P B.W filter,

$$\left|\frac{H(jw)}{A_o}\right| = \frac{1}{\sqrt{1+\left(\frac{w}{w_n}\right)^{2n}}}$$

12. Explain OP-AMP Higher Order Filter

For n[th] order filter, roll-off rate $= -n \times 20$ dB/decode

$$H(s) = \frac{A_{o1}}{s^2+\alpha_1 s+1}\cdot\frac{A_{o2}}{s^2+\alpha_1 s+1}\cdot\frac{A_o}{s+1}$$

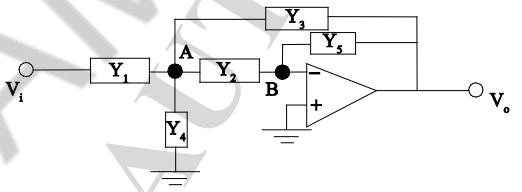
Band Pass Filter

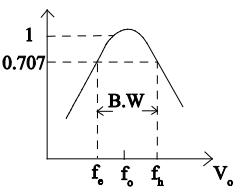
i) Narrow BPF (Q > 10)

ii) Wide BPF (Q < 10)

$$Q_o = {}^{f_o}\!/\!_{BW} = \frac{f_o}{f_h - f_s} \Rightarrow f_o = \sqrt{f_h f_s}$$

Narrow BPF:





The circuit has 2 F/B path and the op-amp is used in inverting mode of operation.

Nodal voltage eq at node A,

$$(V_A - V_i)Y_1 + (V_A - V_B)Y_2 + V_A V_4 + (V_A - V_0)Y_3 = 0$$

$$V_A(Y_1 + Y_2 + Y_3 + Y_4) = V_i V_1 + V_0 Y_3 \qquad [\text{Since } V_B = 0]$$

Nodal voltage eq. at node B,

$$(V_B - V_A)Y_2 + (V_B - V_0)Y_5 = 0$$

$$-V_A Y_2 - V_0 Y_5 = 0$$

$$V_A = -V_0(Y_5/Y_2) \qquad 2$$

Sub 2 in 1

$$-V_0(Y_5/Y_2)(Y_1 + Y_2 + Y_3 + Y_4) = V_i Y_1 + V_0 Y_3$$

$$V_i Y_1 = V_0\left[-Y_3 - \frac{Y_5}{Y_2}(Y_1 + Y_2 + Y_3 + Y_4)\right]$$

$$V_i Y_1 = V_0\left[\frac{-Y_3 Y_2 - Y_1 Y_5 - Y_2 Y_5 - Y_3 Y_5 - Y_4 Y_5}{Y_2}\right]$$

$$\frac{V_0}{V_1} = -\left[\frac{Y_1 Y_2}{Y_2 Y_3 + Y_1 Y_5 + Y_2 Y_5 + Y_3 Y_5 + Y_4 Y_5}\right]$$

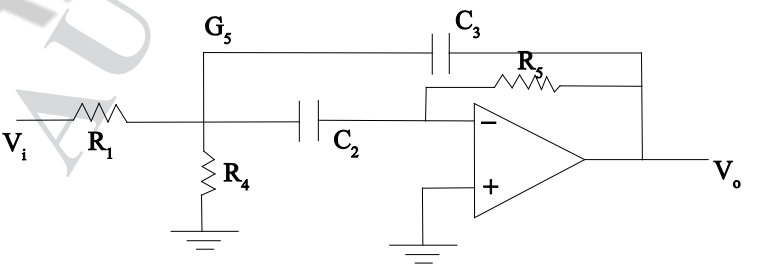
Put $Y_1 = G_1$

$Y_2 = SC_2$

$Y_3 = SC_3$

$Y_4 = G_4$

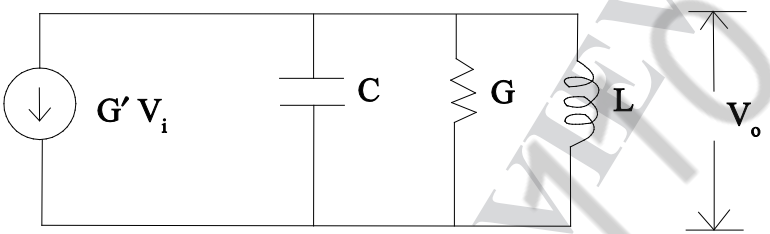
$Y_5 = G_5$



$$H(s)=\frac{V_o(s)}{V_i(s)}=\frac{-sG_1C_2}{s^2C_2C_3+s(C_2+C_3)G_5+G_5(G_1+G_4)}$$

$$H(s)=\frac{G_1}{sC_3+G_5(C_2+C_3)C_2+(G_1+G_4)G_5/sC_2} \qquad 3$$

Eq 3 is equivalent to the gain expression of parallel RLC circuit.



The gain expression is

$$\frac{V_o(s)}{V_i(s)}=-\frac{G'}{Y}=\frac{-G'}{SC+G+\frac{1}{SL}} \qquad 4$$

Compare 3 and 4

$$G'=G_1$$

$$L=\frac{C_2}{G_5(G_1+G_4)}$$

$$G=\frac{G_5(C_2+C_3)}{C_2} \qquad 5$$

$$C=C_3$$

At resonance,

$$w_o{}^2=\frac{1}{LC}=G_5\frac{(G_1+G_4)}{C_2C_3} \qquad 6$$

The gain at resonance,

$$\left.\frac{V_o}{V_i}\right|_{w=w_o}=-\frac{G'}{G}=\frac{-G1}{G}=\frac{-(G_1/G_5)C_2}{C_2+C_3}$$

$$= \frac{-(R_5/R_1)C_2}{C_2 + C_3} \qquad 7$$

Q factor at resonance, $C_2 + C_3$

$$Q_o = \frac{w_o L}{R} = w_o Rc = \frac{w_o c}{G} = \frac{w_o C_2 C_3}{(C_2 + C_3)G_5} \qquad 8$$

$$BW = f_h - f_l = \frac{f_o}{Q_o} = \frac{w_o}{2\pi Q_o} = \frac{w_o}{2\pi R w_o C}$$

$$= \frac{1}{2\pi RC} = \frac{G}{2\pi C} = \frac{G_5(C_2 + C_3)}{2\pi C_2 C_3} \qquad 9$$

Centre frequency $f_o\sqrt{f_h f_e}$ 10

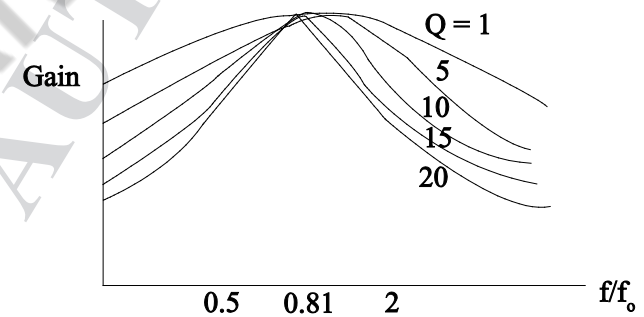
For $C_2 = C_3 = C$, gain at resonant frequency,

$$\left.\frac{V_o}{V_i}\right|_{w=w_o} = \frac{-(R_5/R_1)C}{C + C} = \frac{-(R_5/R_1)C}{2C}$$

$$= -\frac{R_5}{2R_1} = -A_o \qquad 11$$

$$w_o = \frac{\sqrt{G_5(G_1 + G_4)}}{c} \qquad 12$$

$$BW = \frac{}{\pi C} = \frac{}{\pi R\ C} \qquad 13$$



Higher the Q, sharper the filter

Below 0.5fo and above 2fo, all filters roll off at −20 dB/diode independent of Q.

Standard T.F of BPF,

$$H(s)=\frac{-A_o\left(w_o/Q\right)s}{s^2+\left(w_o/Q\right)s+{w_o}^2}=\frac{-A_o\alpha w_o s}{s^2+\alpha w_o s+{w_o}^2} \qquad 14$$

$$\left|H(s)\right|=20\log\left|\frac{A_o\alpha w_o s}{s^2+\alpha w_o s+{w_o}^2}\right|$$

Damping factor $\alpha=\frac{1}{Q}$

Wide BPF:

It is farmed by cascading a HPF & LPF.

If both are of the 1st order, roll-off rate = −20 dB/decode.

$$\left|H_{LP}\right|=\left|\left(1+\frac{R_F}{R_i}\right)\frac{C2\pi fR_2C_2}{1+j2\pi fR_2C_2}\right|=\left|A_{01}\frac{j\left(f/f_1\right)}{1+j\left(f/f_1\right)}\right|$$

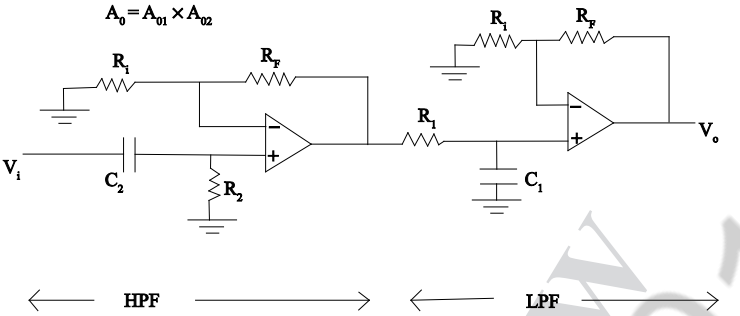
$$=\frac{A_{01}\left(f/f_1\right)}{\sqrt{1+\left(f/f_1\right)^2}}$$

$$f_1=\frac{1}{2\pi R_2C_2}$$

$$\left|H_{LP}\right|=\frac{A_{02}}{\sqrt{1+\left(f/f_1\right)^2}}$$

$$f_1=\frac{1}{2\pi R_1C_1}$$

$$\left|\frac{V_o}{V_i}\right|=\left|\frac{A_0\left(f/f_1\right)}{\sqrt{\left[1+\left(f/f_1\right)^2\right]\left[1+\left(f/f_1\right)^2\right]}}\right|$$



Note:

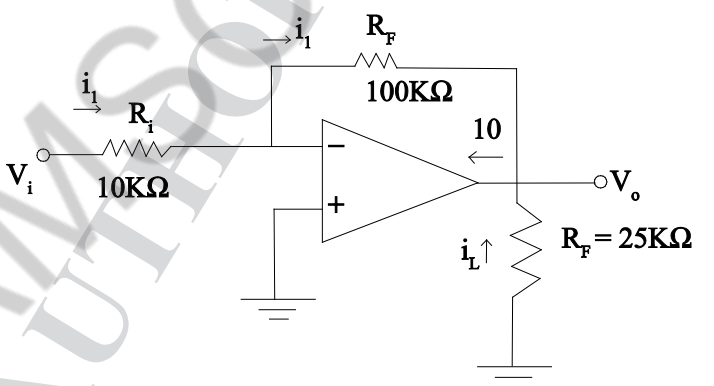
No current can flow into the op-amp input terminals.

$$I_B = 0$$

Due to the concept of mutual ground. 2 input terminals of op-amp are always at the same potential with respect to ground.

13. Given $R_i = 10\ k\Omega$, $R_F = 100\ k\Omega$, $V_1 = 1V$ A load of 25 kΩ is connected to the output terminal calculate.

i) i_1 ii) V_o iii) i_L iv) total current i_o



i) $$i_1 = \frac{V_1}{R_1} = \frac{1V}{10k\Omega} = 0.1mA$$

ii) $$V_o = \frac{R_F}{R_1} V_1 = \frac{-100k\Omega}{10k\Omega}(1V) = -10V$$

iii) $i_L = \frac{V_o}{R_L} = \frac{10V}{25k\Omega} = 0.4 \text{ mA}$

iv) $i_o = i_1 + i_L = 0.1 \text{ mA} + 0.4 \text{ mA} = 0.5 \text{ mA}$

14. A Sine wave of 0.5V peak voltage is applied to an inverting amplifier using R_1 = 10 kΩ, and R_F = 50 kΩ. It uses supply voltages of ±12V. Determine the output and sketch the waveform.

If now the amplitude of input sine wave is increased to 5V, what will be the output Is it practically possible, sketch the waveform?

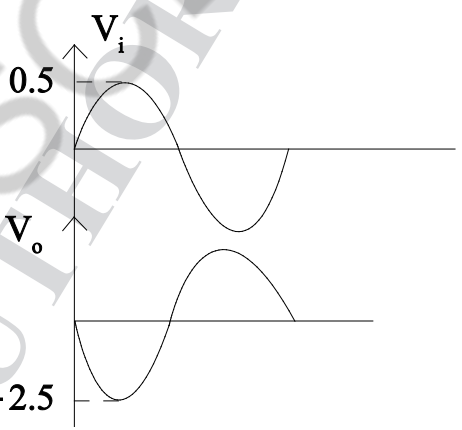
Solution:

a) Given

V_{IN} = 0.5 V, R_1 = 10 kΩ; R_F = 50 kΩ

$$\text{Gain} = \frac{V_o}{V_i} = \frac{-R_F}{R_1}$$

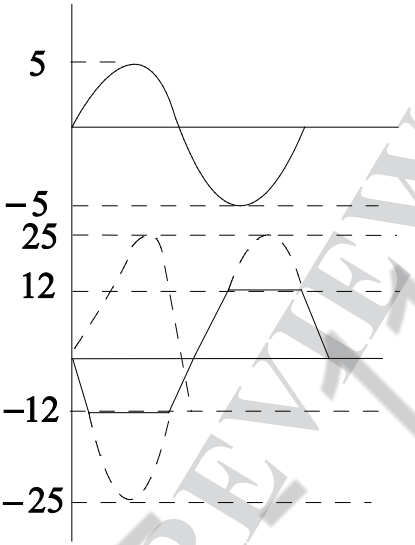
$$\Rightarrow V_o = -(0.5) \times \left(\frac{50}{10}\right) = 2.5\text{v Peak}$$



b) V_{IN} = 5V

$$\text{Gain} = \frac{V_o}{V_i} = \frac{-R_F}{R_1}$$

$$\Rightarrow V_o = -5 \times \left(\frac{50}{10}\right) = 25\text{v Peak}$$



15. For a given OP-AMP ,Let $R_1 = 5\ k\Omega$; $R_F = -20\ k\Omega$, $V_1 = 1V$, $R_L = 5\ k\Omega$

Calculate i) V_o ii) A_{CL} iii) I_L iv) i_o

i) $$\text{Gain} = \frac{V_o}{V_i} = 1 + \frac{R_F}{R_1} \Rightarrow \frac{V_o}{1} = 1 + \frac{20k\Omega}{5k\Omega} \Rightarrow V_o = 5V$$

ii) $$A_{CL} = \frac{V_o}{V_1} = \frac{5}{1} = 5$$

iii) $$i_L = \frac{V_o}{R_L} = \frac{5}{5k\Omega} = 1mA$$

iv) $i_o = i_L + i_1$

$V_1 = 1 - mA$

$i_o = 1mA + 0.2mA$

UNIT - 3

ANOLOG MULTIPLIER AND PLL

PART-A

1. **List the basic building blocks of PLL:**
   1. Phase detector/comparator
   2. Low pass filter
   3. Error amplifier
   4. Voltage controlled oscillator

2. **Define FSK modulation.** **(MAY 2010)**
   FSK is a type of frequency modulation,in which the binary data or code is transmitted by means of a carrier frequency that is shifted between two fixed frequency namely mark (logic 1) and space frequency (logic 0).

3. **What is analog multiplier?** **(MAY2010)**
   A multiplier produces an output v_0, which is proportional to the product of two inputs V_x and V_y $V_0 = kV_xV_y$

4. **List out the various methods available for performing for analog multiplier.**
   - Logarithmic summing technique
   - Pulse height /width modulation technique
   - Variable transconductance technique
   - Multiplication using gilbert cell
   - Multiplication technique using transconductance technique

5. **Mention someareas where PLL is widely used.**
   (DEC 2009)(April/May 2015)
   1 .Radar synchronizations
   2. Satellite communication systems

3. Air borne navigational systems
4. FM communication systems
5. Computers.

6. What are the three stages through which PLL operates?

1. Free running
2. Capture
3. Locked/ tracking

7. Define lock-in range of a PLL. (MAY 2010)

The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock-in range or tracking range. It is expressed as a percentage of the VCO free running frequency.

8. Define capture range of PLL. (MAY 2010)

The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. It is expressed as a percentage of the VCO free running frequency.

9. Define Pull-in time.

The total time taken by the PLL to establish lok is called pull-in time.It depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics

10. Write the expression for FSK modulation. (MAY 2010)

$\Delta vf=f2-f1/k0$

11. Define free running mode. (MAY 2010)

An interactive computer mode that allows more than one user to have simultaneous use of a program.

12. For perfect lock, what should be the phase relation between the incoming signal and VCO output signal?

The VCO output should be 90 degrees out of phase with respect to the input signal.

13. Give the classification of phase detector:

1. Analog phase detector .
2. Digital phase detector

14. What is a switch type phase detector?

An electronic switch is opened and closed by signal coming from VCO and the input signal is chopped at a repetition rate determined by the VCO frequency.This type of phase detector is called a half wave detector since the phase information for only one half of the input signal is detected and averaged.

15. What are the problems associated with switch type phase detector?

1. The output voltage Ve is proportional to the input signal amplitude. This is undesirable because it makes phase detector gain and loop gain dependent on the input signal amplitude.

2. The output is proportional to cosφ making it non linear.

16. What is a voltage controlled oscillator?

Voltage controlled oscillator is a free running multivibrator operating at a set frequency called the free running frequency.This frequency can be shifted to either side by applying a dc control voltage and the frequency deviation is proportional to the dc control voltage.

17. Define Voltage to Frequency conversion factor.

Voltage to Frequency conversion factor is defined as,

Kv = fo / Vc= 8fo /Vcc

Vc is the modulation voltage fo frequency shift

18. What is the purpose of having a low pass filter in PLL?

- It removes the high frequency components and noise.
- Controls the dynamic characteristics of the PLL such as capture range, lock-in range,band-width and transient response.
- The charge on the filter capacitor gives a short- time memory to the PLL

19. Discuss the effect of having large capture range.

The PLL cannot acquire a signal outside the capture range, but once captured, it will hold on till the frequency goes beyond the lock-in range.Thus , to increase the ability of lock range,large capture range is required.But, a large capture range will make the PLL more susceptible to noise and undesirable signal.

20. Mention some typical applications of PLL:

- Frequency multiplication/division
- Frequency translation
- AM detection
- FM demodulation
- FSK demodulation.

21. What is a compander IC? Give some examples.(DEC 2009)

The term companding means compressing and expanding.In a communication system, the audio signal is compressed in the transmitter and expanded in the receiver.

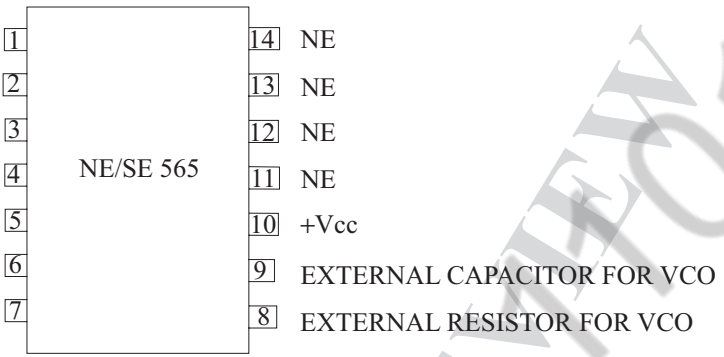
Examples : LM 2704- LM 2707 ; NE 570/571.

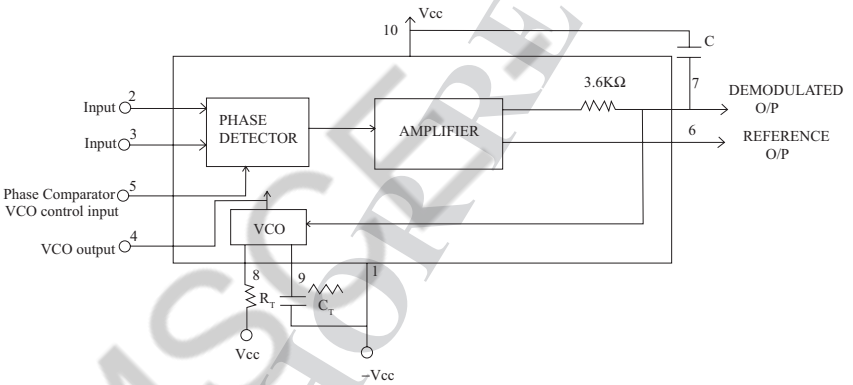
22. What are the merits of companding?

- The compression process reduces the dynamic range of the signal before it is transmitted.
- Companding preserves the signal to noise ratio of the original signal and avoids non linear distortion of the signal when the input amplitude is large.
- It also reduces buzz,bias and low level audio tones caused by mild interference.

PART-B

1. Draw the PLL pin diagram and internal block diagram of PHASE LOCKED loop:





2. Derivation of Lock-in Range of PLL

If Ø is the phase difference between the signal and VCO voltage, output voltage of analog phase detector given by

$$\theta_e = K_\phi \left(\phi - \frac{\pi}{2} \right)$$

$$\theta_e = AK_\phi \left(\phi - \frac{\pi}{2} \right)$$

A voltage gain of the amplifier

K_ϕ Linear angle to voltage transfer co-off

Shifts VCO frequency from its frequency to the frequency f given by

$$f = f_o + K_\theta V_c$$

when PLL is locked

$$f = f_s = f_o + K_\theta V_c$$

$$V_c = \frac{f_s - f_o}{K_{\grave{e}}} = AK_\phi\left(\phi - \frac{\pi}{2}\right)$$

$$\text{Thus} \quad \phi = \frac{\pi}{2} + \left(f_s - f_o\right)/K_v K_\phi A$$

Error voltage is maximum for $\emptyset = 0$ or π

$$\theta_{e(max)} = \pm\left(\frac{\pi}{2}\right)K_\phi$$

$$\theta_{c(max)} = \pm\left(\frac{\pi}{2}\right)K_\phi A$$

Maximum VCO frequency swing is given by

$$\left(f - f_o\right)_{max} = K_\theta V_{c(max)}$$

$$= K_\theta K_\phi A\left(\frac{\pi}{2}\right)$$

$$f_s = f_o + K_\theta V_{c(max)}$$

$$= f_o + K_\theta K_\phi A\left(\frac{\pi}{2}\right) = f_o \pm \Delta f_L$$

$$\Delta f_L \quad K_\theta K_\phi A\left(\frac{\pi}{2}\right)$$

$$2\Delta \quad K_\theta K_\phi A\pi$$

$$K_\theta = \frac{8f_o}{V}$$

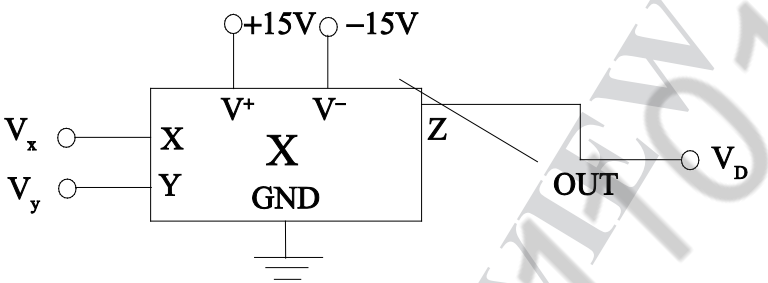
$$V = +Vcc - (-Vcc)$$

$$K_\phi = \frac{14}{\pi} \qquad \& \quad A = 14$$

$$\Delta f_L = \frac{8f_o}{V} \quad \frac{1.4}{\pi} \; 1.4(\pi)$$

$$\Delta f_L = \frac{\pm 7.8 f_o}{V}$$

3. Explain about Analog Multiplier:



$$V_o = \frac{V_x V_y}{V_{ref}}$$

Analog multiplier produces an output V_o, which is proportional to the product of two inputs V_x and V_y

$V_o = K V_x V_y$

Where K = scaling factor

$$K = \frac{1}{V_{ref}} = \left(\frac{1}{10}\right) V^{-1}$$

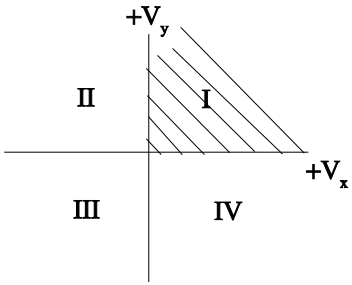
$$V_o = \frac{V_x V_y}{V_{ref}} \quad (\text{or}) \quad V_o = \frac{V_x V_y}{10}$$

Quadrant:

The quadrant define the applicability of the circuit for bipolar signals at its input.

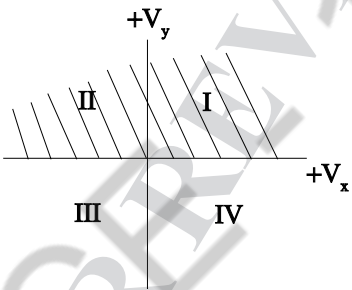
One Quadrant Multiplier:

If both inputs are positive IC is said to be one quadrant multiplier.



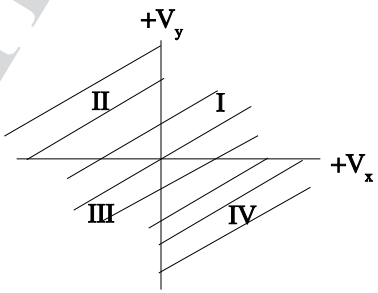
Two Quadrant Multiplier:

If one input is hold positive, other is bound to both positive and negative then it is said to be two quadrant multiplier.



Four Quadrant multiplier:

If both inputs may be positive or negative, the IC is called four quadrant multiplier.



4. Explain any two Methods for Analog Multiplication

i) Logarithmic summing technique

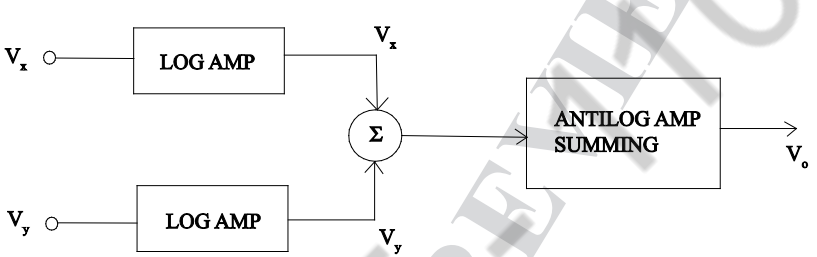
ii) Pulse height/width modulation technique

iii) Variable trans conductance technique

iv) Multiplication using gilbert all

v) Multiplication using variable trans conductance technique

Logarithmic Summing Technique:



$V_x + V_y - (V_x V_y)$

The output of summer is given to analog amplifier.

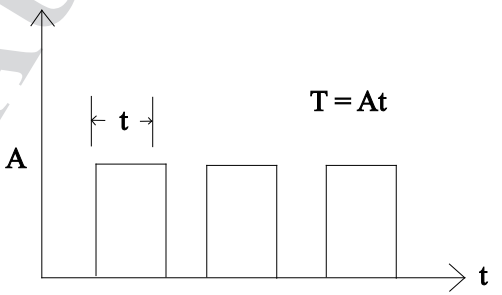
$$V_o = \text{in}\left[\text{in}\left(V_x V_y\right)\right]$$

$$V_o = \frac{V_x V_y}{V_{ref}}$$

Log amp requires the input and reference voltage to be of same polarity.

So, this type of multiplier can be used for only one quadrant multiplication.

Pulse Height/Width Modulation Technique:



In this method, pulse width is proportional to one input voltage and pulse amplitude is proportional to the other input voltage.

V1=K1t

V2=K2A

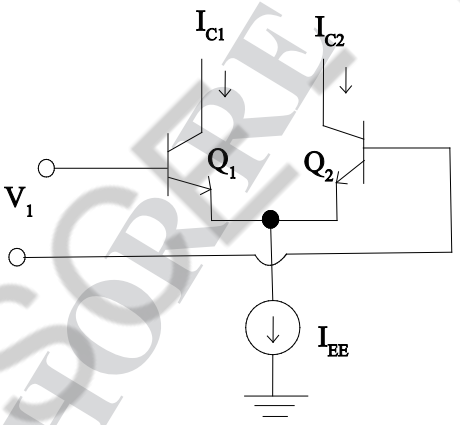
Where t=width of pluse

A= Amplitude of Pluse, Now the output is the product of the two inputs.

Vz=KV1V2

Thus the output is proportional to the area of pulse, which in term is proportional to the product of two input voltages.

5. Explain the Multiplier Using An Emitter Coupled Transistor Pair:



The output current I_c, and I_{c2} are related to the differential input voltage V_1 by

$$I_{c1} = \frac{I_{EE}}{1+e} V_i / V_T$$

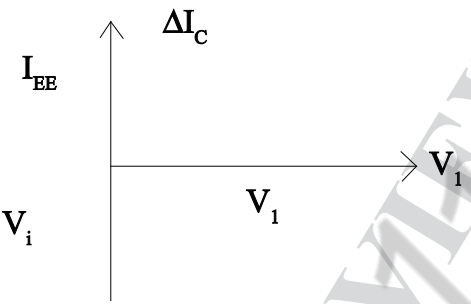
$$I_{c2} = \frac{I_{EE}}{1+e} V_i / V_T$$

V_T = thermal voltage

$$\Delta I_c = I_{c1} - I_{c2}$$

$$I_{EE} = \left[\frac{1}{1+e^{-Vi/VT}} - \frac{1}{1+e^{+Vi/VT}}\right]$$

$$\Delta I_c = I_{EE} \tan\left(\frac{V_i}{V_T}\right)$$



The transfer characters of emitter coupled pair characters shows that emitter coupled.

When $V_1 << V_T$

$$I_{EE} = \tan\left(\frac{V_i}{2V_T}\right) = I_{EE}\left(\frac{V_i}{2V_T}\right)$$

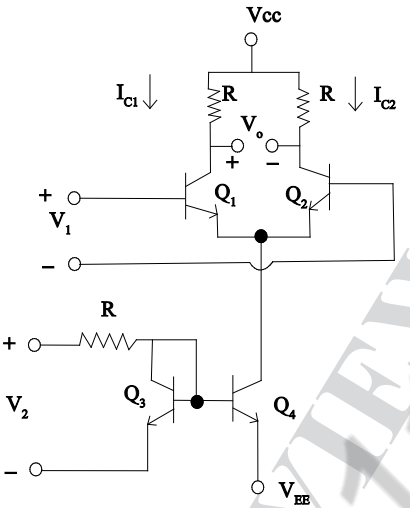
$$\Delta I_c \simeq I_{EE}\left(\frac{V_i}{2V_T}\right) \qquad 1$$

I_{EE} = bias current for emitter coupled pair. If current I_{EE} is made proportional to a second input signal V_2, then

$$I_{EE} \simeq K_o\left(V_2 - V_{BE(ON)}\right) \qquad 2$$

Put 2 in 1

$$\Delta I_c = \frac{K_o V_1\left(V_2 - V_{BE(ON)}\right)}{2V_T}$$



Limitations:

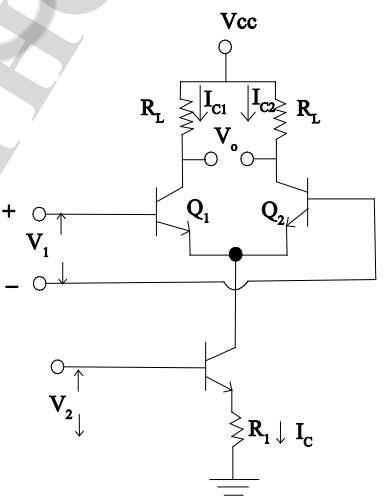
V_2 is offset by $V_{BE(ON)}$

V_2 must always be positive which results in only two quadrant multiplication.

$\tan h(x) = X$

where $X = \frac{V_1}{2V_T}$

6. Explain the Variable Trans conductance Technique:



Differential amplifier is formed by transistors Q_1 and Q_2

When $V_1 << V_T$

$$V_o = I_m R_L V_1 \qquad 1$$

$$\text{Where } I_m = \frac{I_E}{V_T} \qquad 2$$

I_E is controlled by V_2

If $I_E R_E >> V_{BE}$

$V_2 = I_E R_E$

$$\therefore \quad I_E = \frac{V_2}{R_E} \qquad 3$$

Sub 3 in 2

$$I_m = \frac{V_2}{R_E V_T} \qquad 4$$

Sub 4 in 1

$$V_o = \frac{V_2 V_1 R_L}{R_E V_T} = \left(\frac{R_L}{R_E V_T}\right) V_1 V_2$$

$$V_o = K V_1 V_2$$

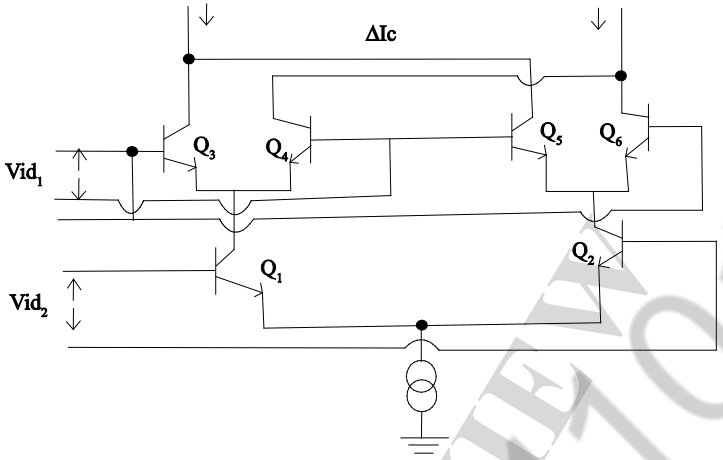
This the output is proportional to the product of 2 output voltages.

Limitations:

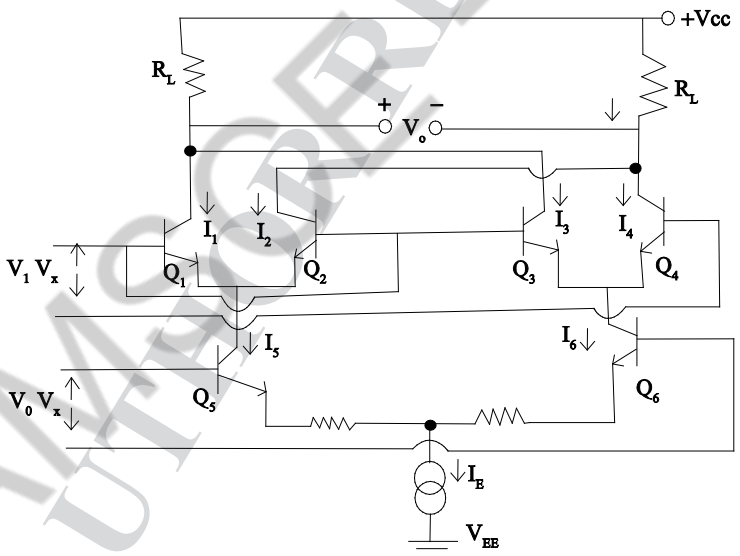
Scale factor K is temperature dependent.

In varies is a functions of voltage V_2.

These problems can be eliminated using cell.



Emitter coupled pair $Q_1 - Q_2$ is in series with cross coupled emitter coupled pairs ($Q_3 - Q_6$). IEE – Emitter Bias current for Q1 and Q2.



The outputs a V_1 and V_2 these inputs determine the diagram of total analog various branches.

Assume,

i) All the transistors are well matched

ii) h_{fe} of the transistor is very high

ie $h_{fe} >> 1$

$I_1 + I_2 = I_5$

$I_3 + I_4 = I_6$

$I_5 + I_6 = I_E$

Assume $|V_i| << V_T$,

$I_1 - I_2 = (T_m)_{12} V_1$ 1

$I_B - I_4 = (T_m)_{34} V_1$ 2

Where $(T_m)_{12}$ & $(T_m)_{34}$ are transconductance of the transistor pair$(Q_1 - Q_2)$ & $(Q_3 - Q_4)$.

Under the absence of emitter degeneration resistance.

$$(T_m)_{12} = \frac{I_5}{V_T}$$

$$(T_m)_{34} = \frac{I_6}{V_T}$$

$\therefore$ V_o $Rc\left[(I_1 - I_2) - (I_3 - I_4)\right]$ 3

Sub 1 & 2 in 3

V_o $R_L\left[(T_m)_{12} V_1 - (T_m)_{34} V_1\right]$

$$R_1 V_1 \left|\frac{I_5}{V_T} - \frac{I_6}{V_T}\right|$$

V_0 $R_1 V_1 |I_5 - I_6|$

$V_o = K V_1 V_2$

Limitations:

V_1 should be lesser than V_T. If $V_1 > V_T$, the transistor pairs $Q_1 - Q_2$ & $Q_3 - Q_4$ will function as a switch which turn ON and OFF depending upon the polarity of V_1. Thus this circuit will act as a switch rather than a linear multiplier.

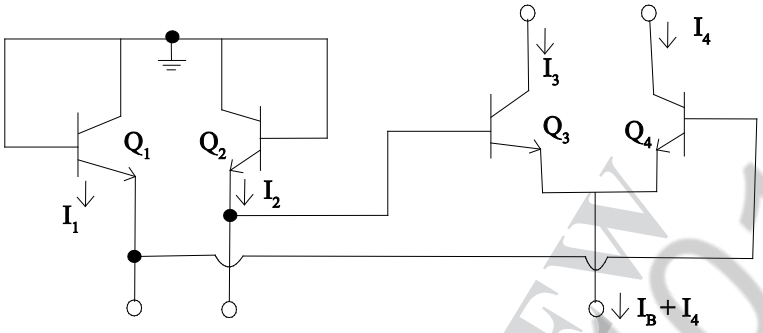
Four Quadrant Variable Transconductance Multiplier:

This circuit consist of

i) Linearized transconductance multiplier

ii) Differential V – I converter.

Linearized Transconductance Multiplier:



$(Q_3 - Q_4)$ will act as variable transconductance amplifier.

$(Q_1 - Q_2)$ used as diode with base collector shorted.

Applying KV_1 to the pair $(Q_1 - Q_2)$ & $(Q_3 - Q_4)$

$$V_{BE3} + V_{BE4} = V_{BE1} + V_{BE2}$$

$$V_{BE3} - V_{BE4} = V_{BE1} - V_{BE2}$$

For the two matched transistors, change in V_{BE} is proportional to the log ratio of their currents.

Hence $\Delta V_{BE} \alpha \text{ in}\left(\frac{I_1}{I_2}\right)$

$$\text{in}\left(\frac{I_3}{I_4}\right) = \text{in}\left(\frac{I_1}{I_2}\right)$$

$$\frac{I_3}{I_4} = \frac{I_1}{I_2}$$

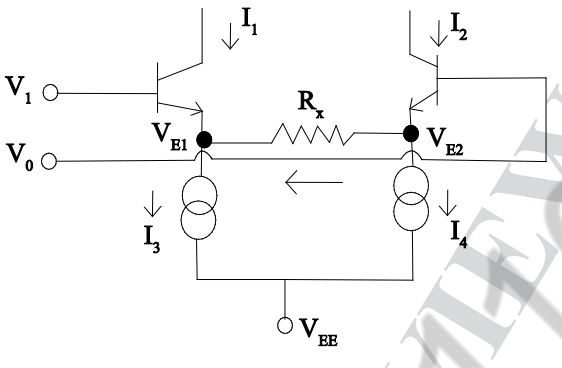
$$\frac{I_3 - I_4}{I_3 + I_4} = \frac{I_1 - I_2}{I_1 + I_2}$$

$$(I_3 - I_4) = \frac{(I_1 - I_2)(I_3 + I_4)}{(I_1 + I_2)}$$

To get $(I_1 + I_2)$ & $(I_3 + I_4)$ from the input voltages V_1 and V_2, two V – I converters are necessary and to convert $(I_3 - I_4)$ to the output voltage V_o one I – V converter is must.

7. Explain Differential V – I Converter:

To convert input voltage to get differential current, V – I converter is used.



Neglecting uses

$I_1 = I_x + I_{Rx}$

$I_2 = I_x - I_{Rx}$

$I_1 - I_2 = 2I_{Rx}$

$$I_{Rx} = \frac{V_{E1} - V_{E2}}{Rx}$$

$$\therefore \quad I_1 - I_2 = \frac{2(V_{E1} - V_{E2})}{Rx}$$

$V_{E1} = V_1 - V_{BE1}$

$V_{E2} = V_2 - V_{BE2}$

$V_{E1} - V_{E2} = (V_1 - V_2) - (V_{BE1} - V_{BE2})$

$$\Delta V_{BE} \ \alpha \ \text{in}\left(\frac{I_1}{I_2}\right)$$

$$V_{E1} - V_{E2} = (V_1 - V_2) - V_T \ \text{in}\left(\frac{I_1}{I_2}\right)$$

$$\therefore \quad I_1 - I_2 = \frac{2}{Rx}(V_1 - V_2) - \frac{2V_T}{Rx} \ \text{in}\left(\frac{I_1}{I_2}\right)$$

$$I_1 - I_2 = \frac{2}{Rx}(V_1 - V_2)$$

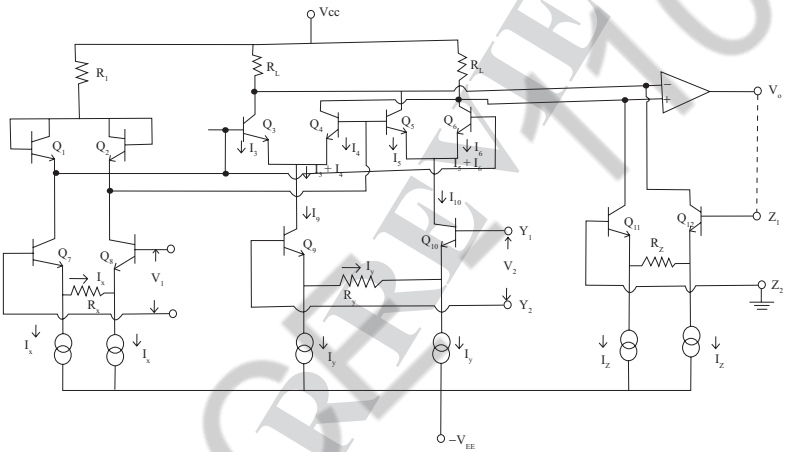
Thus the circuit performs V – I conversion.

8. Discuss the Four Quadrant Multiplier Circuit:

The linearized trans conductance multiplier operates only over two quadrants. Hence using little modifications and using differential V – I converter four quadrant variable transconductance multiplier circuit is obtained.

If uses i) 2 linearized transconductance pairs

ii..V – I converters



Op-amp along with 3rd V – I converter of transistors Q_{11} and Q_{12} forms the output I – V converter.

Applying KVL,

$$V_B = Vcc - R_L (I_3 + I_5 + I_{12})$$

$$V_A = Vcc - R_L (I_4 + I_6 + I_{11})$$

For op-amp $V_A = V_B$

$$Vcc - R_L (I_3 + I_5 + I_{12}) = Vcc - R_L (I_4 + I_6 + I_{11})$$

$$I_3 + I_5 + I_{12} = I_4 + I_6 + I_{11}$$

$$(I_4 + I_6) - (I_3 + I_5) = (I_{12} + I_{11})$$

$$(I_{12} + I_{11}) = \frac{2}{Rz}(Z_1 - Z_2)$$

$$\frac{2}{Rz}(Z_1 - Z_2) = \frac{2(Y_1 - Y_2)(X_1 - X_2)}{I_x R_z R_y}$$

$$(Z_1 - Z_2) = K(X_1 - X_2)(Y_1 - Y_2)$$

where $K = \dfrac{Rz}{I_x R_z R_y}$

Let $V_1 = X_1 - X_2$

$V_2 = Y_1 - Y_2$

$V_x = Z_1 - Z_2$

$V_z = K\, V_1 V_2$

For linearized converter,

$$(I_3 - I_4) = \frac{(I_1 - I_2)(I_3 + I_4)}{(I_1 + I_2)} \qquad 1$$

For V – I converter,

$$(I_1 - I_2) = \frac{2}{Rx}(X_1 - X_2) \qquad 2$$

Sub 2 in 1

$$(I_3 - I_4) = \frac{2(I_3 + I_4)(X_1 - X_2)}{Rx(I_1 + I_2)} \qquad 3$$

$$\left.\begin{aligned} I_1 + I_2 &= 2Ix \\ I_3 + I_4 &= I_9 \end{aligned}\right\} \qquad 4$$

Sub 4 in 3

$$(I_3 - I_4) = \frac{2\, I_9 (X_1 - X_2)}{2R_x I_x} \qquad 5$$

$$I_5 + I_6 = I_{10}$$

$$I_6 - I_5 = \frac{I_{10}(X_1 - X_2)}{I_x R_x} \qquad 6$$

Subtract 5 from 6

$$(I_6 - I_5) - (I_3 - I_4) = \frac{(X_1 - X_2)}{I_x R_x}(I_{10} - I_9) \qquad 7$$

Q_9 and Q_{10} forms V – I converter

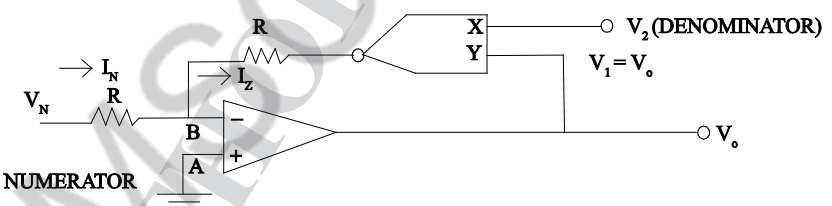
$$(I_{10} - I_9) = \frac{2}{Rx}(Y_1 - Y_2) \qquad 8$$

Sub 8 in 9

$$(I_4 + I_6) - (I_3 - I_5) = \frac{(Y_1 - Y_2)(X_1 - X_2)}{I_x R_y R_x}$$

9. Explain the analog multiplier's Applications

(i) Voltage Divider:



The circuit in which the output is the diversion of 2 input signals is called as a voltage divider.

Denominator is applied at the X input. Numerator is applied at the input terminal.

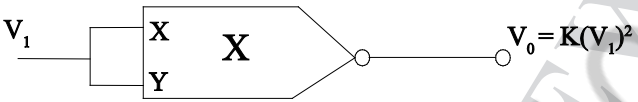
$$I_v = I_z = \frac{V_N}{R} = \frac{-V_Z}{R}$$

$$V_z = K\,V_1\,V_2 = KV_oV_2$$

$$\frac{V_N}{R} = \frac{-KV_o V_Z}{R}$$

$$V_o = \frac{-V_Z}{KV_2}$$

(ii) Squaring Circuit:



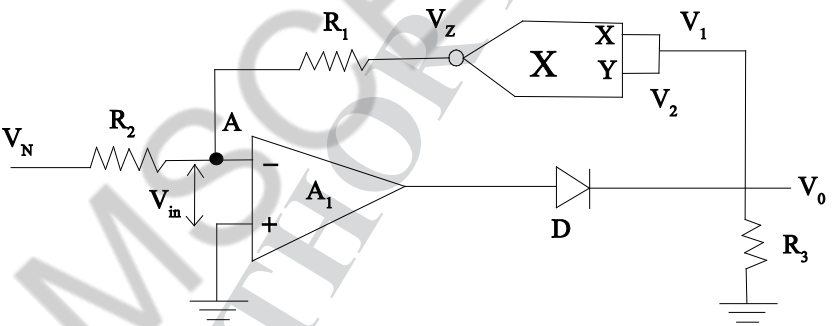
Squaring circuit gives square of the input signal applied.

$$V_o = KV_1V_2$$

Here $V_1 = V_2$

$$V_o = KV_1$$

(iii) Square Rooting Circuit:



Let the gain of an op-amp A_1 is A

So, $V_o = -V_{in}A$

$$V_{in} = \frac{-V_o}{A} \qquad 1$$

Apply KCL at node A

$$\frac{V_{in} - V_N}{R_2} + \frac{V_{in} - V_z}{R_1} = 0$$

$$V_{in} = V_N\left(\frac{R_1}{R_1+R_2}\right)+V_z\left(\frac{R_2}{R_1+R_2}\right)$$

where $V_z = KV_1V_2$

$$V_z = KV_1^2$$

$$V_z = KV_o^2$$

$$V_{in} = V_N\left(\frac{R_1}{R_1+R_2}\right)+K\,V_o^2\left(\frac{R_2}{R_1+R_2}\right) \qquad 2$$

Equate 1 & 2

$$\frac{-V_o}{A} = V_N\left(\frac{R_1}{R_1+R_2}\right)+K\,V_o^2\left(\frac{R_2}{R_1+R_2}\right)$$

$$V_o^2 = \left[\frac{-V_o}{A}-V_N\left(\frac{R_1}{R_1+R_2}\right)\right]\left(\frac{R_1+R_2}{R_2}\right)\left(\frac{1}{R}\right)$$

$$V_o^2 = \frac{-V_o}{A}\left(\frac{R_1+R_2}{R_2}\right)\left(\frac{1}{R}\right)-V_N\left(\frac{R_1}{R_2}\right)\left(\frac{1}{R}\right)$$

$$V_o^2 = -V_N\left(\frac{R_1}{KR_2}\right)\left(\frac{1+V_o(R_1+R_2)}{V_NAR_1}\right)$$

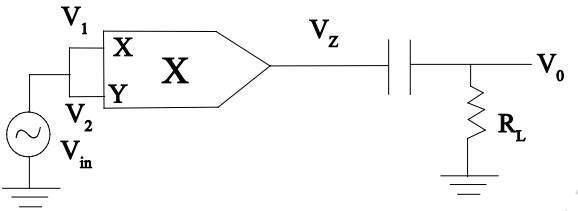
$$\frac{V_o(R_1+R_2)}{V_NAR_1} << 1$$

$$V_o^2 = (-V_N)\frac{R_1}{KR_2}$$

$$V_o = \sqrt{(-V_N)\frac{R_1}{KR_2}}$$

To perform square root operation, V_N must always be negative. Otherwise the circuit will be latched up and normal operation can be performed by breaking the feedback loop. To avoid such problem series diode is used.

Frequency Doubler:



$V_1 = V_m \text{ Sinwt}$

$V_2 = V_{2m} \text{ Sin}(wt + \theta)$

$V_o = KV_1V_2$

$V_o = KV_{1m} V_{2m} \text{ Sinwt Sin}(wt + \theta)$

$V_o = KV_{1m} V_{2m} \text{ Sinwt [Sin wt Cos } \theta + \text{ Cos wt Sin } \theta]$

$V_o = KV_{1m} V_{2m} [\text{Sin}^2 \text{ wt Cos } \theta + \text{ Sinwt Cos wt Sin } \theta]$

$$\left[\text{sinwtcoswt} - \frac{\text{sin2wt}}{2}\right]$$

$$\text{sinwt} - \frac{1-\cos 2wt}{2}$$

$$V_o = KV_{1m} V_{2m} \left[\left(\frac{1-\cos 2wt}{2}\right)\cos\theta + \frac{\text{sin2wt}}{2}\sin\theta\right]$$

$$V_o = \frac{KV_{1m} V_{2m}}{2}\left[\cos\theta - \cos\theta \cos 2wt + \sin\theta \sin 2wt\right]$$

$$V_o = \underbrace{\frac{KV_{1m} V_{2m}}{2}\cos\theta}_{\text{DC term}} - \underbrace{\frac{KV_{1m} V_{2m}}{2}\cos(2wt - \theta)}_{\text{varies with time}}$$

When $V_1 = V_2 = V_{in} = V_m \sin wt$

$$V_z = K(V_{in})^2 = K(V_m \sin wt)^2$$

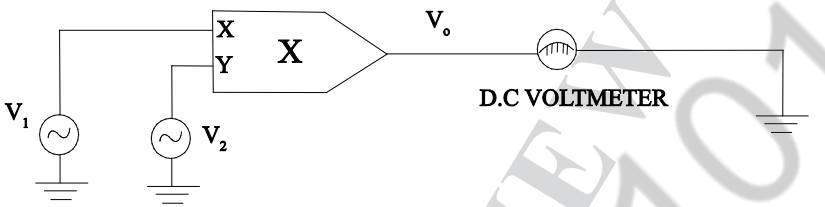
$$= KV_m^2\left(\frac{1-\cos 2wt}{2}\right)$$

$$V_z = \frac{KV_m^2}{2} - \frac{KV_m^2}{2} \cos 2wt$$

Capacitor c will black the DC

So, $V_o = \frac{KV_m^2}{2} (\cos 2wt)$

Phase Angle Detection:



output of multiplier is

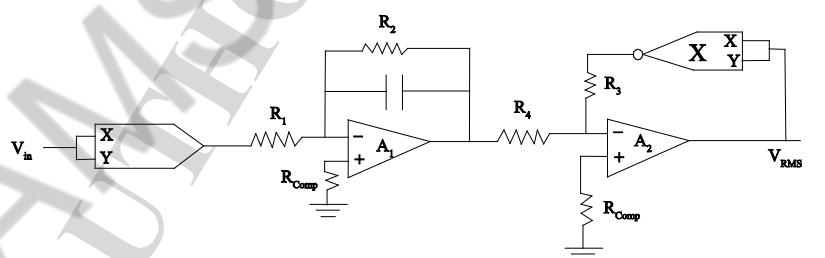
$$V_o = \frac{KV_{1m}V_{2m}\cos\theta}{2} = KV_{1m}V_{2m}\cos(2wt - \theta)$$

DC voltmeter will not respond to AC components.

For $\theta - 0°$, voltmeter reading $= \frac{KV_{1m}V_{2m}}{2}$

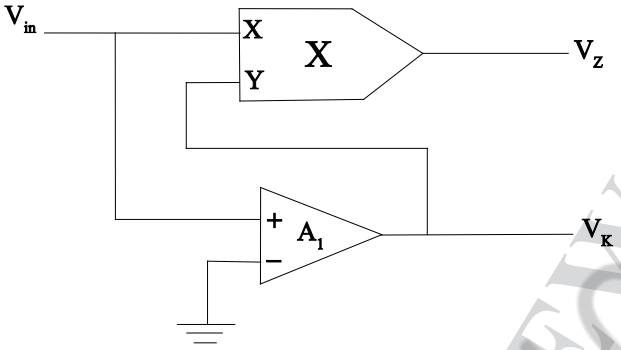
$\theta - 45°$, voltmeter reading $= \frac{KV_{1m}V_{2m}}{\sqrt{2}}$

RMS Detector:



First the input is given to the squaring circuit and then given to the integrator. Finally op-amp A_z along with multiplier performs square rooting operation. Thus the final value is the RMS value of the input signal applied.

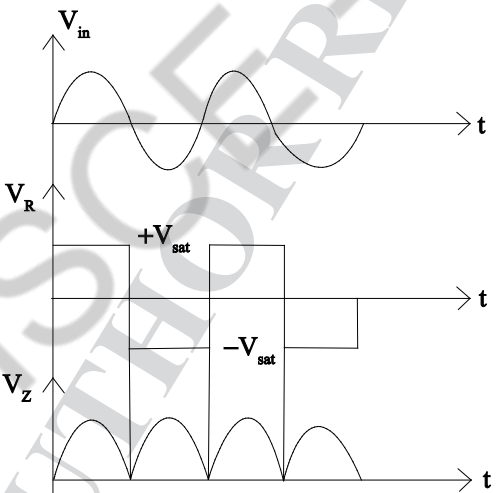
Rectifier:



Op-amp A_1 is used as non-inverting comparator.

output of op-amp A_1 is $V_k = \pm V_{sat}$ depends on V_{in}.

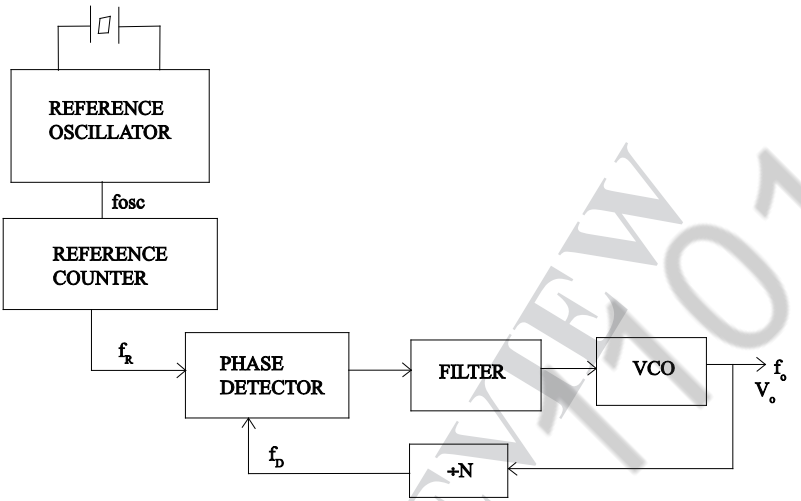
Full wave rectified signal is obtained at V_Z.



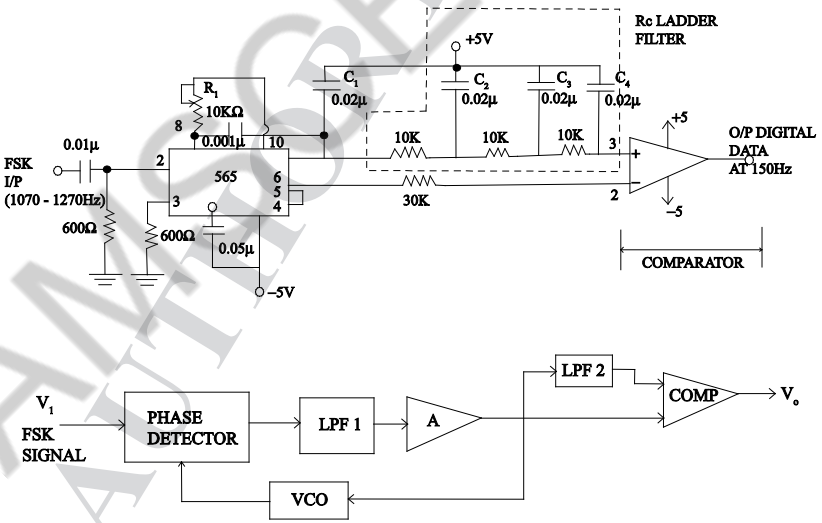
$$\Delta V_f = \frac{f_e - f_i}{K_o}$$

The reference voltage for the comparator is derived from the additional LPF and it is adjusted midway between V_{f1} and V_{f2}, comparator give is output 0 and 1.

10. Discuss the Frequency Synthesizer & FSK demodulators



Frequency Shift Keying (FSK) Demodulation:



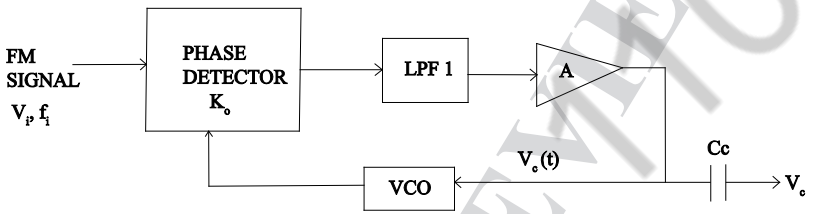
PLL is designed to remain in back with the FSK signal for both the frequencies f_1 and f_2.Within the PLL is lacked with f_1, VCO ,Control voltage is given by

$$V_{f1} = \frac{f_i - f_e}{K_o}$$

When the PLL is locked with f_2,

$$_{f2} \quad \underline{f_c \quad f_o}$$

11. Explain AM &FM Detection and Frequency Translation



The instantaneous frequency of the input signal is given by,

$$f_i(t) = f_c + \Delta f_c \ \sin w_m t$$

f_c = carrier frequency

Δf_c = peak frequency deviation

w_m = angular frequency of the modulating signal.

When the PLL is locked, VCO frequency will be equal to the instantaneous frequency of the input signal.

$$f_i(t) = f_c + K_o \ V_c$$

$$V_c = \frac{f_i(t) - f_c}{K_o}$$

$$V_c = f_i(t) \frac{f_c + \Delta f_c \sin w_m(t) - f_c}{K_o}$$

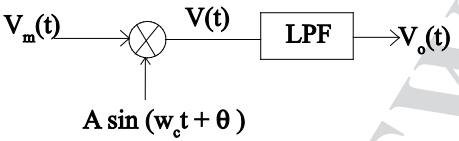
$$V_c = \frac{\Delta f_c \sin w_m(t)}{K_o}$$

Thus the FM signal gets demodulated. The control voltage of VCO is a linear function of instantaneous frequency deviation.

The Centre frequency to should be set as close as possible to the FM corner frequency f_o to achieve maximum lock range.

PLL can be used as an AM detector for demodulating the amplitude modulated signals.

Assume the AM signal is given by,



$$V_m(t) = V_p\left[1 + m(t)\sin w_c t\right]$$

$$V(t) = V_m(t) A \sin\left(w_c t + \theta\right)$$

$$V(t) = A\, V_p\left[1 + m(t)\right]\sin w_c t \sin\left(w_c t + \theta\right)$$

$$V(t) = A\, V_p\left[1 + \frac{m(t)}{2}\right]\left[\cos\left(w_c t - w_c t - \theta\right) - \cos\left(w_c t + w_c t + \theta\right)\right]$$

$$V(t) = A\, V_p\left[1 + \frac{m(t)}{2}\right]\left[\cos(\theta) - \cos\left(2w_c t + \theta\right)\right]$$

Higher frequency term will be eliminated by LPF

$$V(t) = A\, V_p\left[1 + \frac{m(t)}{2}\right]\cos\theta$$

$$V(t) = V\left[1 + m(t)\cos\theta\right]$$

This application can be implemented using PLL.

Here the oscillator signal is locked to the carrier frequency of the input signal.

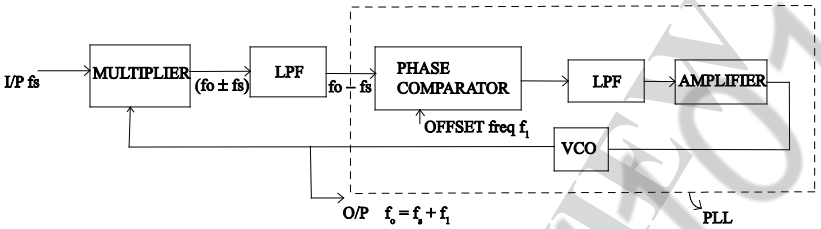
Under locked condition, VCO output is 90° out of phase with the input signal. AM input signal is 90° phase shifted before applied to the multiplier.

Hence the two input's applied to the multiplier are now in phase. output of multiplier is passed to LPT to filter high frequency components and the output is thus directly proportional to the amplitude of input signal.

Frequency Translation:

Shifting the input frequency by a small factor is called as frequency translation.

Multiplier and LPF are connected external to PLL.



f_s and f_o are given to multiplier output of multiplier is $(f_o \pm f_s)$

Sum component will be removed by LPF and only the difference component $(f_o - f_s)$ is given as one of the input to the phase comparator. Other input is f_1

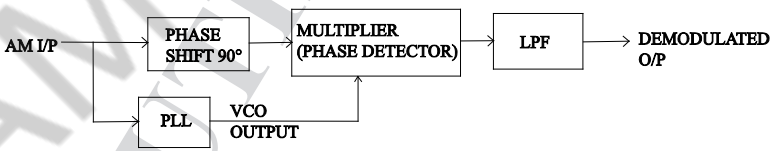
When PLL is locked

$f_o - f_s = f_1$

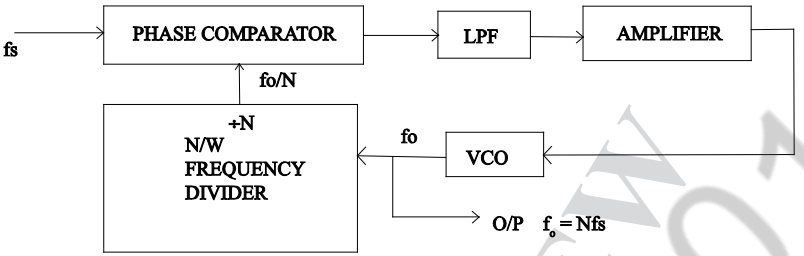
$f_o = f_s + f_1$

Thus the input frequency f_s is shifted by a small factor f_1

AM Detection:



12. Explain the Applications of PLL as Frequency Multiplication/Division:



A divide by N network is inserted between phase comparator and VCO.

Multiplication factor can be obtained by selecting a factor scaling factor by

When the PLL is locked,

$$f_s = — \quad \Rightarrow \quad \therefore \quad f_o = Nf_s$$

Multiplication can also be done without using the frequency divider network for which the input signal should such in harmonies. In this n^{th} harmonic of input signal will be locked to the VCC output

$$nf_s = f_o$$

Since the amplitude of higher order harmonics becomes less, locking can't takes place. [n < 10]

Same circuit can also be used to perform division for which m^{th} harmonic of VCC output should be locked to input signal.

$$mf_o = f_s \quad \Rightarrow \quad f_o = \frac{f_s}{m}$$

UNIT - 4

ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERTERS

PART-A

1. Name the essential parts of a DAC.(MAY 2010)

- Drive motors
- Analog devices
- Deglitcher
- Filter

2. Write down the drawback of weighted D/A converter.

The main disadvantage of binary weighted D/A converter is the requirement of wide range of resister values.As the length of the binary word is increased .the range of resister values needed also increases.

3. List the broad classification of ADCs.

1. Direct type ADC.
2. Integrating type ADC.

4. List out the direct type ADCs. (DEC 2009)

1. Flash (comparator) type converter
2. Counter type converter
3. Tracking or servo converter
4. Successive approximation type converter

5. List out some integrating type converters.

1. Charge balancing ADC
2. Dual slope ADC

6. What is integrating type converter?

An ADC converter that perform conversion in an indirect manner by first changing the analog I/P signal to a linear function of time

or frequency and then to a digital code is known as integrating type A/D converter.

7. Explain in brief the principle of operation of successive Approximation ADC.

The circuit of successive approximation ADC consists of a successive approximation register (SAR), to find the required value of each bit by trial & error.With the arrival of START command, SAR sets the MSB bit to 1. The O/P is converted into an analog signal & it is compared with I/P signal. This O/P is low or High. This process continues until all bits are checked.

8. What are the main advantages of integrating type ADCs?

a. The integrating type of ADC's do not need a sample/Hold circuit at the input.

b. It is possible to transmit frequency even in noisy environment or in an isolated form.

9. Where are the successive approximation type ADC's used?

The Successive approximation ADCs are used in applications such as data loggers & instrumentation where conversion speed is important.

10. What is the main drawback of a dual-slop ADC?(DEC 2009)

The dual slope ADC has long conversion time. This is the main drawback of dual slope ADC

11. State the advantages of dual slope ADC(DEC 2009)

It provides excellent noise rejection of ac signals whose periods are integral multiples of the integration time T.

12. Define conversion time.(DEC 2009)

It is defined as the total time required to convert an analog signal into its digital output. It depends on the conversion technique used & the propagation delay of circuit components.

The conversion time of a successive approximation type ADC is given by

$$T(n+1)$$

where T---clock period

T_c---conversion time

n----no. of bits

13. Define resolution of a data converter. (MAY 2010)

The resolution of a converter is the smallest change in voltage which may be produced at the output or input of the converter.

Resolution (in volts)= VFS/2^n-1=1 LSB increment. The resolution of an ADC is defined as the smallest change in analog input for a one bit change at the output.

14. Define accuracy of converter. (MAY 2010)

Absolute accuracy:

It is the maximum deviation between the actual converter output & the ideal converter output.

Relative accuracy:

It is the maximum deviation after gain & offset errors have been removed.

The accuracy of a converter is also specified in form of LSB increments or % of full scale voltage.

15. What is settling time?

It represents the time it takes for the output to settle within a specified band

±½LSB of its final value following a code change at the input (usually a full scale change). It depends upon the switching time of the logic circuitry due to internal parasitic capacitance & inductances. Settling time ranges from 100ns. 10μs depending on word length & type circuit used.

16. Explain in brief stability of a converter:

The performance of converter changes with temperature age & power supply variation . So all the relevant parameters such as offset, gain, linearity error & monotonicity must be specified over the full temperature & power supply ranges to have better stability performances.

17. What is meant by linearity?

The linearity of an ADC/DAC is an important measure of its accuracy & tells us how close the converter output is to its ideal transfer characteristics. The linearity error is usually expressed as a fraction of LSB increment or percentage of full-scale voltage. A good converter exhibits a linearity error of less than ± ½LSB.

18. What is monotonic DAC?

A monotonic DAC is one whose analog output increases for an increase in digital input.

19. What are the specifications of D/A converter?

The specifications are accuracy, offset voltage, monotonicity, resolution, and settling time.

20. What is multiplying DAC?

A. digital to analog converter which uses a varying reference voltage VR is called a multiplying DAC(MDAC). If the reference voltage of a DAC, VR is a sine wave given by

$V(t)=Vin \quad Cos\ 2 \quad ft$

Then, $Vo(t)=V_{om}Cos(2 \quad ft + 180^{o})$

21. What is a sample and hold circuit? Where it is used?

A sample and hold circuit is one which samples an input signal and holds on to its last sampled value until the input is sampled again. This circuit is mainly used in digital interfacing, analog to digital systems, and pulse code modulation systems.

22. Define sample period and hold period. (DEC 2009)

The time during which the voltage across the capacitor in sample and hold circuit is equal to the input voltage is called sample period.The time period during which the voltage across the capacitor is held constant is called hold period.

23. Which is the fastest ADC and why? (MAY 2010)

Simultaneous type A/D converter(flash type A/D converter) is the fastest because A/D conversion is performed simultaneously through a set of comparators .

24. What are the advantages and disadvantages of R-2R ladder DAC?(MAY2010)

Advantage:

- Easier to build
- Number of bits can be expanded by adding more sections.

Disadvantage:

- More power dissipation makes heating, which in turns develops non-linearties in DAC.

25. Give the disadvantages of flash type A/D converter.(MAY 2010)

The simultaneous type A/D converter is not suitable for A/D conversion with more than 3 or 4 digital output bits. Then (2n-1)comparators are required for

an n-bit A/D converter and the number of comparators required doubles for each added bit.

26. Define quantization error.

In A/D converter the smallest digital step is due to the LSB and it can be made smaller only by increasing the number of bits in the digital representation. This error is called quantization error.

27. Define Dither.

It is a very small amount of random noise(white noise) which is added to the input before A/D conversion to improve the performance of A/D converter.

28. Define Delta modulation.

Delta modulation is a technique in which derivative of the signal is quantized. The delta modulation shows slope overload for fast input signals and their performance is dependent on input signal frequency.

29. Define slope overload noise and granular noise.

Slope overload noise is introduced due to the use of a step size delta is too small

To follow some portions of the waveform with a step size.

Granular noise results from using a step size that is too large in parts of the waveform having a small slope.

30. List out the uses of sigma delta A/D converters.

- High resolution
- Moderate speech applications such as digital audio, digital telephony

31. Discuss different Types of DAC:

1. Weighted resistor DAC
2. R – 2R ladder
3. Inverted R – 2R ladder

32. An 8-bit DAC has an output voltage range of 0 – 2.55v. Define its resolution in two ways.

Solution:

$n = 8; \quad V_{OFS} = 2.55v$

$\text{Resolution} = 2^n = 2^8 = 256$

$$\text{Resolution} = \frac{V_{OFS}}{2^n - 1} = \frac{2.55}{256 - 1} = 10mv$$

33. The digital input for a 4-bit DAC is 0110. Calculate its final output voltage.

Solution:

$n = 4$

$V_{OFS} = 15v$

$$\text{Resolution} = \frac{V_{OFS}}{2^n - 1} = \frac{15}{2^4 - 1} = 1v$$

$V_o = \text{resolution} \times D$

$D = \text{decimal of } (0110)_2 = 6$

$V_o = 1 \times 6 = 6v$

34. An 8-bit DAC has resolution of 20mv/LSB. Find V_{OFS} and V_o if the input is $(10000000)_2$

Solution:

$$\text{Resolution} = \frac{V_{OFS}}{2^n - 1}$$

$$20\times10^{-3} = \frac{V_{OFS}}{2^8 - 1}$$

$V_{OFS} = 5.1v$

D = equivalent of $(10000000)_2 = 128$

V_o = Resolution × D = $20 \times 10^{-3} \times 128 = 2.56v$

35. A 12-bit DAC has a step size of 8mv. Determine the full scale output voltage and percentage resolution. Also find the output voltage for the input of 010101101101?

Solution:

n = 4

Step size = −8mv

$V_{OFS} = 8mv \times 2^{12} - 1 = 32.76v$

$$\% \text{ Resolution} = \frac{8mv}{32.76V} \times 100 = 0.02442$$

The output voltage for the input 010101101101 = $8mv \times (1389)_{10}$

= 11.112v

36. An 8-bit D/A converter has a resolution of 10mv/bit find the analog output voltage for the inputs.

(a) 10001010 (b) 00010000

Solution:

D = decimal of $(10001010)_2 = 138$

V_o = Resolution × D = 10mv × 138 = 1.38v

D = decimal of $(00010000)_2 = 16$

$V_o = 16 \times 10mv = 0.16v$

37. How many bits are required to design a D/A converter, that can have a resolution of 5mv? The ladder has +8v full scale.

$$\text{Resolution} = \frac{V_{FS}}{2^n - 1}$$

$$2^n - 1 = \frac{V_{FS}}{\text{Resolution}} = \frac{8}{5\times10^{3}} \Rightarrow 2^n = \frac{8}{5\times10^{-3}} + 1$$

$$2^n = 1601$$

$$\log 2^n = \log 1601$$

$$n \log 2 = \log 1601$$

$$n = \frac{\log 1601}{\log 2} = 10.6447$$

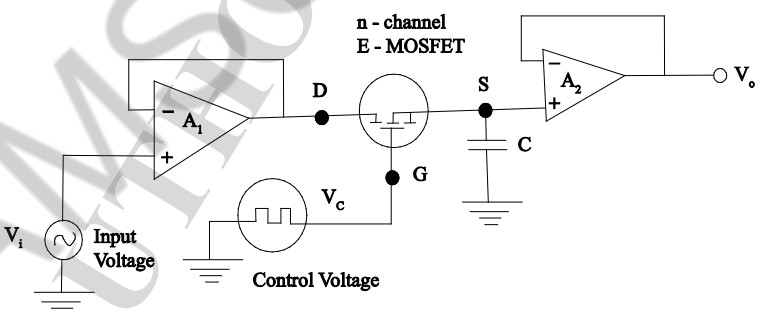
PART-B

1. Explain the Sample and Hold Circuit:

A sample and hold circuit samples an input signal and holds on to its last sampled value until the input is sampled again.

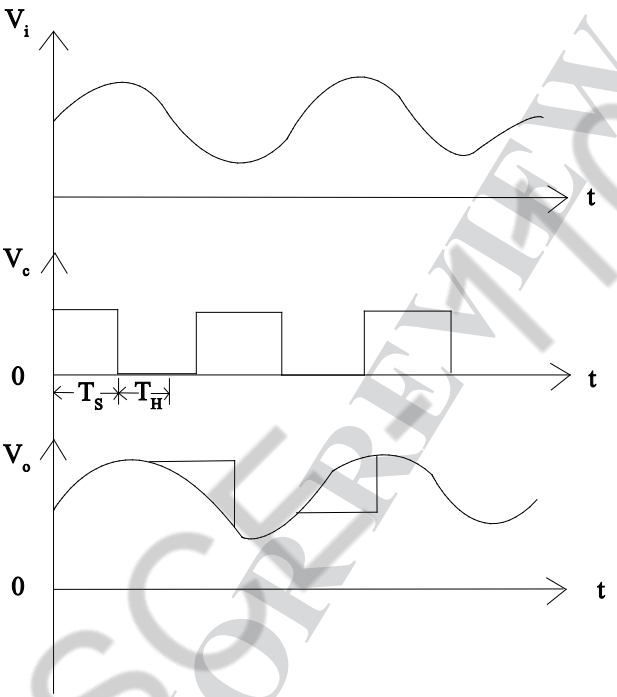
Data Sample and Hold Circuit:

1. Digital interfacing
2. Analog to digital
3. Pulse code modulation systems



The n-channel E-MOSFET works as a switch and is controlled by the control voltage V_c and the capacitor C stores the charge. The analog signal V_i to be sampled is applied to the drain of E-MOSFET and control voltage V_c is applied to its gate.

When V_c is positive, the E-MOSFET turns on and the capacitor C charges to the instantaneous value of input V_i with a time constant C. The input voltage V_i appears across the capacitor C and then at the output through the voltage follower A_2.



When control voltage V_c is zero, the E-MOSFET is off. The capacitor C is at high input impedance of the voltage follower A_2 and capacitor holds the voltage. The time period T_s, the time during which voltage across the capacitor is equal to input voltage is called sample period. The time period T_H of V_c during which the voltage across the capacitor is held constant is called hold period.

The frequency of the control voltage should be kept higher than the input so as to retrieve the input from output waveform. A low leakage capacitor such as polystyrene, Mylar or Teflon should be used to retain the stored charge.

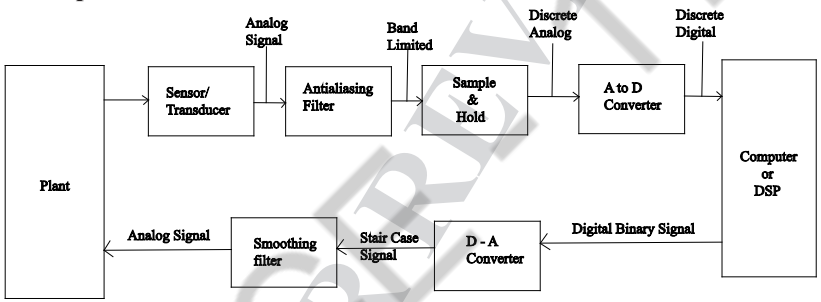
$$H(s) = \frac{A_o s^2}{s^2\left[1 + {}^{w_1}\!/_{s}\,(3 - A_o) + \left({}^{w_1}\!/_{s}\right)^2\right]}$$

$$H(s) = \frac{A_o}{1 + {}^{w_1}\!/_{s}\,(3 - A_o) + \left({}^{w_1}\!/_{s}\right)^2}$$

For $s = 0$; $H(o) = 0$

$s = \infty$; $H(\infty) = A_o$ so the circuit acts as the High pass filter.

2. Explain the D – A Converters:



Physical quantities such as voltage, current, temperature, pressure and time etc., are available in analog form.

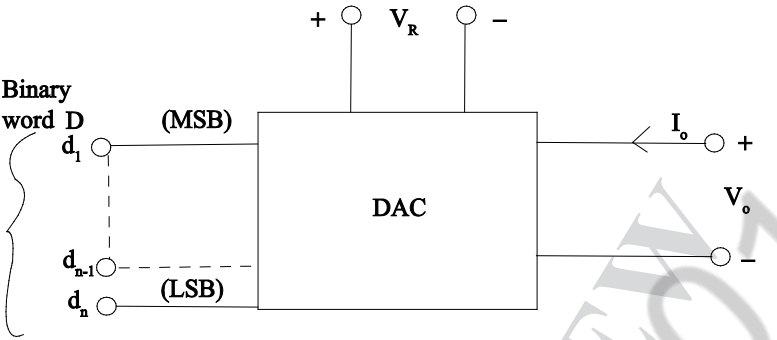
H is difficult to process, transmit and store the parameters in analog form due noise, error.

So digital form is preferred for its better accuracy and reduced noise.

Applications:

1. Digital audio recording and playback
2. Computer
3. Music and Video Synthesis
4. Data Acquisition
5. Digital Multimeter
6. Digital Signal Processing
7. Microprocessor Based Instrumentation

DAC Techniques:



The input is an n-bit binary word D and is combined with a reference voltage V_R to give an analog output signal.

The output DAC can be either a voltage or current.

For voltage output DAC, the D/A converter is mathematically expressed as

$$V_o = K\, V_{FS}\left(d_1 2^{-1} + d_2 2^{-2} + ...d_n 2^{-n}\right) \qquad 1$$

Where,

V_o = output voltage

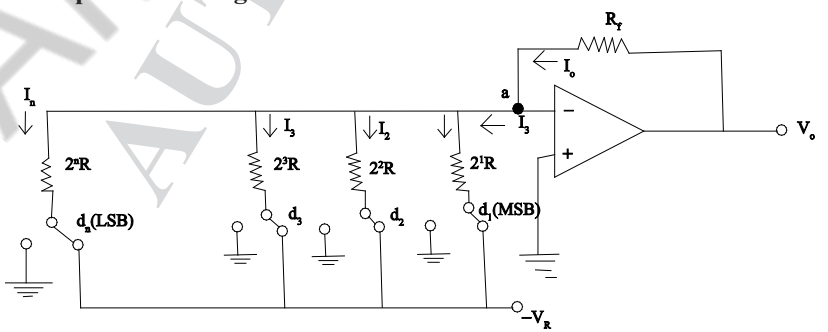
V_{FS} = Full scale output voltage

K = Scaling factor

d_1 = Most significant (MSB) with weight of $V_{FS}/2$

d_n = LSB with of $V_n/2$

3. Explain the Weighted Resistor DAC:



The simplest circuit that uses a summing amplifier with a binary weighted resistor network. It has n – electronic switches d_1, d_2, …….. d_n. Controlled by binary input word. These switches are single pole double throw (SPOT) type.

If the binary input to a particular switch is 1, it connects the resistance to the reference voltage ($-V_R$) and if the input bit is 0, the switch connects the resistor to the ground.

The output current I_o for an op-amp is

$$I_o = I_1 + I_2 + \ldots\ldots I_n$$

$$= \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \ldots\ldots \frac{V_R}{2^n R} d_n$$

$$= \frac{V_R}{R}\left(d_1 2^{-1} + d_2 2^{-2} + \ldots\ldots d_n 2^{-n}\right) \qquad 1$$

The output voltage

$$V_o = I_o R_f$$

$$= V_R \frac{R_f}{R}\left(d_1 2^{-1} + d_2 2^{-2} + \ldots\ldots d_n 2^{-n}\right) \qquad 2$$

Comparing 1 & 2

If $R_f = R$

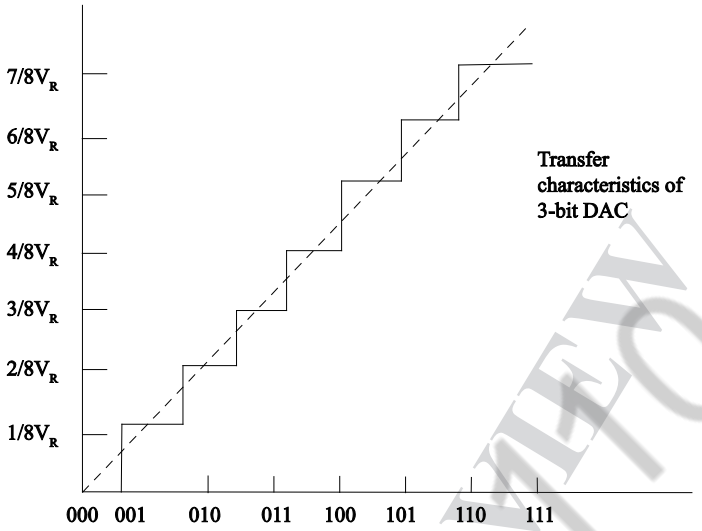
$$V_{FS} = V_R$$

$$K = 1$$

The circuit uses a negative reference voltage. So the analog output voltage is positive staircase. The op-amp is simply working as a current to voltage converter. The accuracy and stability of a DAC depends upon the accuracy of the resistors and the tracking of each other with temperature.

The disadvantages of binary weighted type DAC is the wide range of resistors values required.

Different types of SPDT electronic switches are available (i) A totem pole MOSFET switch (ii) CMOS inverter switch.



Performance Parameters of DAC:

Resolution is the number of different analog output values that can be provided by a DAC.

For an n-bit DAC

Resolution $= 2^n$

Resolution $= \frac{V_{OFS}}{2^n - 1}$; % Resolution $= \frac{\text{Stepsize}}{V_{FS}} \times 100$

Where V_{OFS} = Full scale output voltage

Accuracy:

It is a comparison of actual output voltage with expected output. H is expressed in percentage (%).

Accuracy $= \frac{V_{OFS}}{(2^n - 1)2}$

Stability:

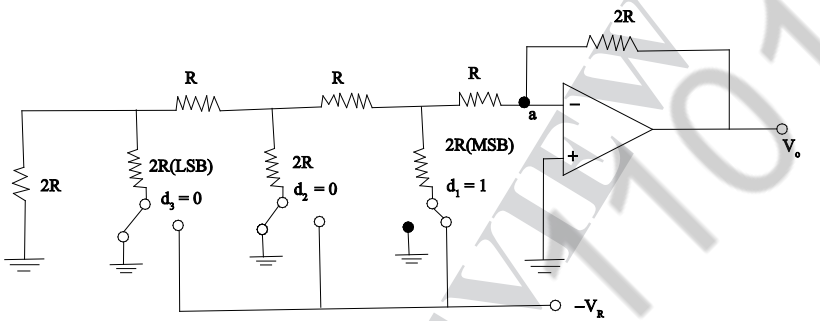
1. Settling time
2. Monotonicity

4. Describe the R – 2R Ladder DAC:

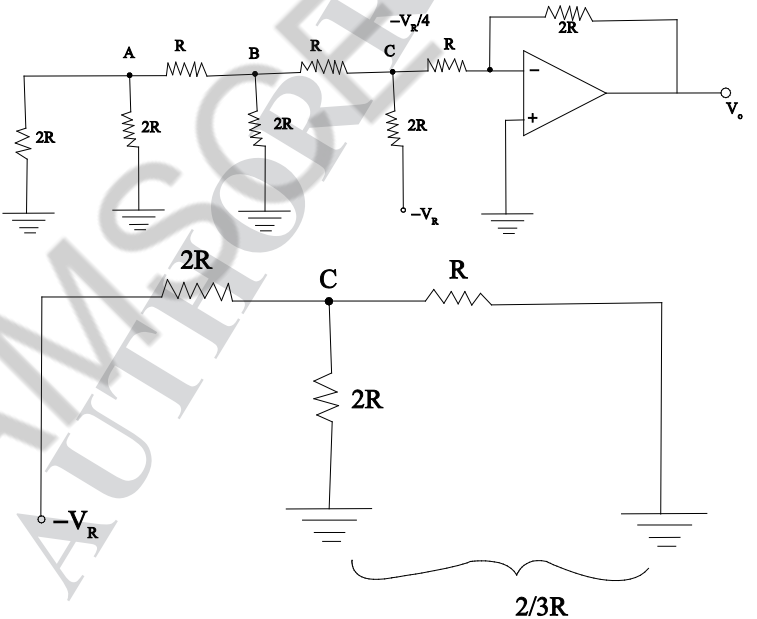
Wide range of resistors are required in binary weighted resistor type DAC.

This can be avoided by using R – 2R ladder type DAC where only two values of resistors are required.

The typical value of R. Ranges from 2.5KΩ to 10KΩ.



Consider a 3 – bit DAC, where the switch position $d_1d_2d_3$ corresponds to the binary word 100.



Voltage at node c can be easily calculated by the set procedure of network analysis as

$$\frac{-V_R\left(\frac{2}{3}R\right)}{2R+\frac{2}{3}R}=\frac{-V_R\left(\frac{2}{3}R\right)}{\frac{6R+2R}{3}}=\frac{-V_R\,2R}{48R}=\frac{-V_R}{4}$$

The output voltage

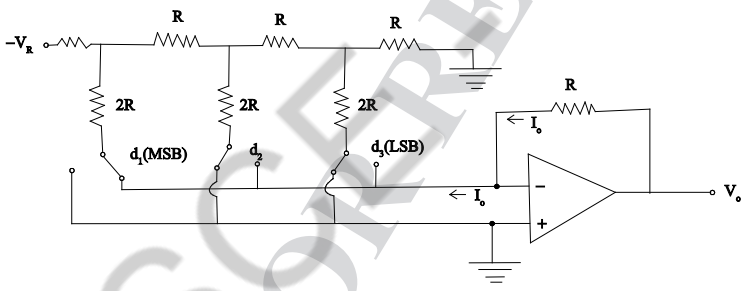
$$V_o=\frac{-2R}{R}\left(\frac{-V_R}{4}\right)=\frac{V_R}{2}=\frac{V_{FS}}{2}$$

5. Explain the Inverted R – 2R Ladder:

In weighted resistor type DAC and R – 2R ladder type DAC, current flowing in the resistors changes as the input date changes.

More power dissipation causes heating, which in turn, creates non-linearity in DAC.

This can be avoided completely in inverted R – 2R ladder type DAC.



A 3-bit inverted R – 2R ladder type. DAC, where the position of MSB and LSB is interchanged.

Each input binary word connects the corresponding switch either to ground or to the inverting input terminal of the op-amp which is also at virtual ground.

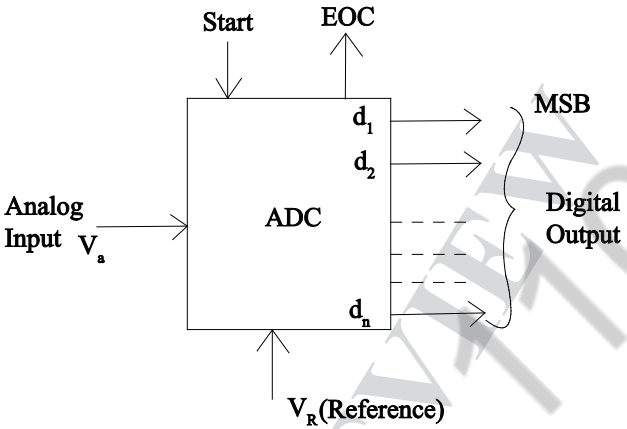
Since both the terminals of switches d_i are at ground potential, current flowing in the resistances is constant and independent of switch position.

When switch d_i is at logical '0', the current through 2R resistor flows to the ground and when the switch d_i is at logical '1', the current through 2R sinks to the virtual ground.

The circuit has the important property that the current divides equally at each of the nodes.

This is because the equivalent resistance to the right or to the left of any node is exactly 2R.

6. Explain different A/D Converter:



The ADC provides the function opposite of a DAC.
It accepts an analog input voltage V_a and produces an output binary word d_1, d_2…..d_n of functional value D.

$$D = d_1 2^{-1} + d_2 2^{-2} + ... + d_n 2^{-n}$$

where $d_1 \rightarrow$ MSB

$d_n \rightarrow$ LSB

An ADC usually has two additional control lines.

1. START input – To tell the ADC when to start conversion.
2. EOC (End of Conversion) – output to announce when the conversion is complete.

ADCs are classified broadly classified into

(i) Direct type ADCs

(ii) Integrating type ADCs

1. Flash (Comparator) type converter
2. Counter type converter
3. Tracking or servo converter
4. Successive approximation type converter

Integrating Type ADCs are

1. Charge balancing ADC
2. Dual slope ADC

Successive approximation ADCs are used in

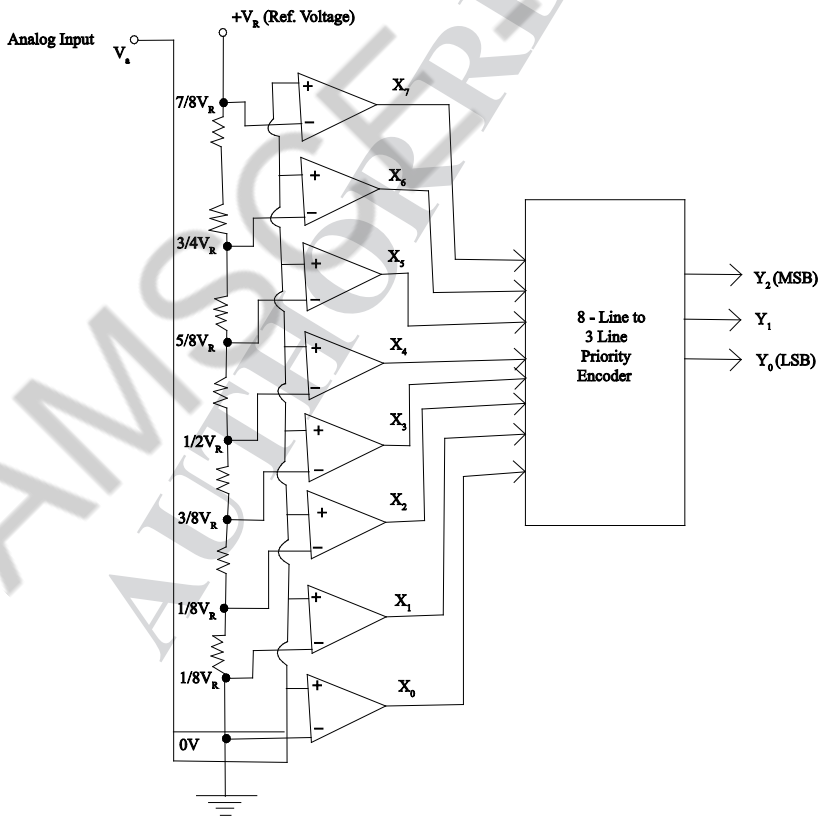
1. Data loggers
2. Instrumentation

Integrating types are used in

1. Digital meter
2. Panel meter
3. Monitoring systems

7. With circuit diagram , explain Flash type ADCs:

Flash (Parallel Comparator) A/D Converter:



It is a simplest, fastest and most expensive A/D technique. The circuit consist of a resistive divider network, 8 op-amp comparators and a 8-line to 3-line encoder. A small amount of hysteresis is built into the comparator to resolve any problems that might occur if both inputs were of equal voltage.

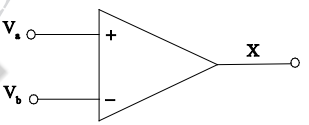
At each node of the resistive divider, a comparison voltage is available. Since all the resistors are of equal value, the voltage levels available at the nodes are equally divided between the reference voltage V_R and the ground. The purpose of the circuit is to compare the analog input voltage V_a with each of the node voltages.

The circuit has the advantage of high speed as the conversion take place simultaneously rather than sequentially. Typical conversion time is 100 ns or less. Conversion time is limited only by the speed of the comparator and the priority encoder.

Disadvantages:

The no. of comparators required doubles for each added bit.

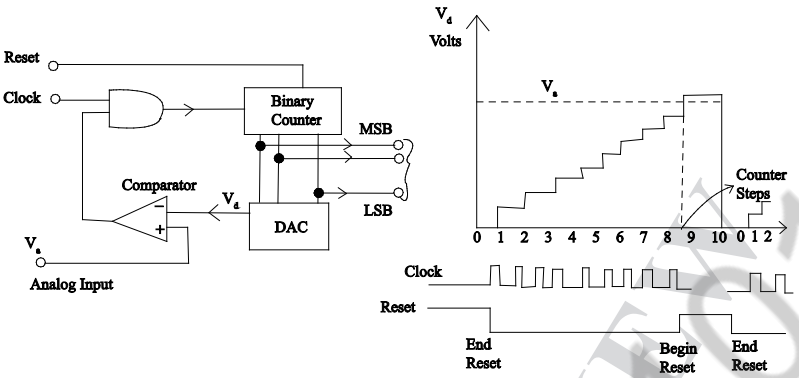
Voltage Input	Output X
$V_a > V_d$	X = 1
$V_a < V_a$	X = 0



Flash type A/D Converter Truth Table:

Input	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$V_R/8$ to $V_R/4$	0	0	0	0	0	0	1	1	0	0	1
$V_R/4$ to $3V_R/8$	0	0	0	0	0	1	1	1	0	1	0
$3V_R/8$ to $V_R/2$	0	0	0	0	1	1	1	1	0	1	1
$V_R/2$ to $5V_R/8$	0	0	0	1	1	1	1	1	1	0	0
$5V_R/8$ to $3V_R/4$	0	0	1	1	1	1	1	1	1	0	1
$3V_R/4$ to $7V_R/8$	0	1	1	1	1	1	1	1	1	1	0
$7V_R/8$ to V_R	1	1	1	1	1	1	1	1	1	1	1

8. Explain Counter Type A/D Converter:



The D to A converter can easily be turned around to provide the inversion function A to D conversion. The principle is to adjust the DAC's input code until the DAC's output comes within ±1/2 LSB to the analog input V_a which is to be converted to binary digital form. This can be done by a 3-bit counting ADC.

The counter is reset to zero count by the reset pulse. Upon the release of RESET, the clock pulses are counted by the binary counter. These pulses go through the AND gate which is enabled by the voltage comparator high output. The no. of pulses counted increase with time. The binary word representing this count is used as the input of a D/A converter whose output is staircase. The analog output V_d of DAC is compared to the analog input V_a by the comparator.

If $V_a > V_d$, the output of the comparator becomes high and the AND gate is enabled to allow the transmission of the clock pulses to the counter.

If $V_a < V_d$, the output of the comparator becomes low and the AND gate is disabled.

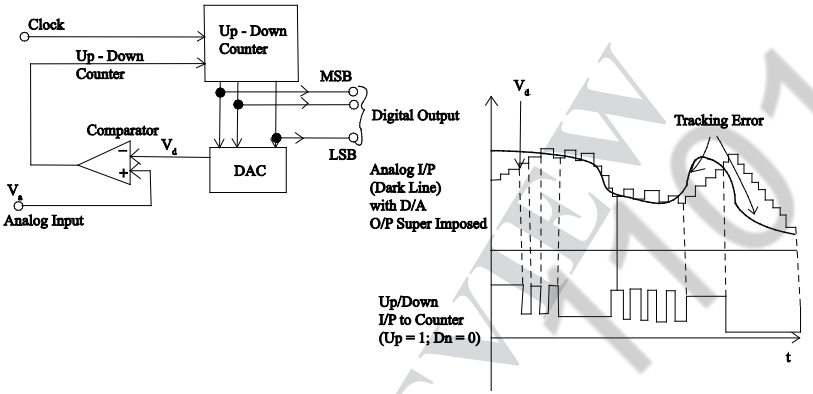
This stops the counting at the time $V_a \leq V_d$. For new value of V_a, a second reset pulse is applied to clear the counter. At the end of the reset, the counting begins again. The counter frequency must be low enough to give sufficient time for the DAC to settle and for the comparator to respond.

Disadvantage:

Low speed

The conversion time can be as long as $(2^n - 1)$ clock periods depending upon the magnitude of input voltage V_a.

9. With neat diagram, explain Servo Tracking A/D Converter:



An improved version of counting ADC is the tracking or a servo converter. The circuit consists of an up/down counter with the comparator controlling the direction of the count. The analog output of the DAC is V_d and is compared with the analog input V_a. If the input V_a is greater than the DAC output signal, the output of the comparator goes high and the counter is caused to count up.

The DAC output increases with each incoming clock pulse and counts down. This causes the control to control up and the count increases by ±1LSB around the correct value. As long as the analog input changes slowly, the tracking A/D will be within one LSB of the correct value. However, when the analog input changes rapidly, the tracking A/D cannot keep up with the change and error occurs.

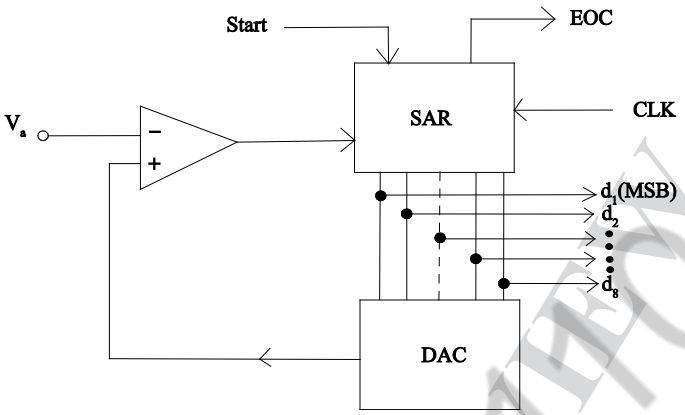
Advantage:

Very simple

Disadvantage:

The time needed to stabilize as the new conversion value is proportional to the rate at which the analog signal changes.

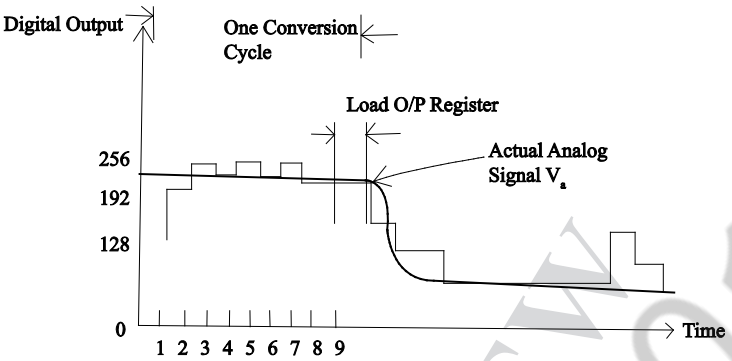
10. Explain the Successive Approximation Converter:



The successive approximation technique uses a very efficient code search strategy to complete n-bit conversion in just n – clock periods. An eight bit converter would require eight clock pulses to obtain a digital output. The circuit uses a successive approximation register (SAR) to find the required value of each bit by trial and error.

With the arrival of the START command, the SAR sets the MSB $d_1 = 1$ with all other bits to zero so that code is 10000000. The output V_d of the DAC is compared with analog input V_a. If V_a is greater than the DAC output V_d than 10000000, is less than the correct digital representation. The MSB is left at '1' and the next LSB is made.

If $V_a < V_d$, then 10000000 is greater than the correct digital representation. The MSB is left at '0' and the next to LSB is made '0'. This procedure is repeated for all subsequent bits, one at a time until all bit positions have been tested. Whenever the DAC output crosses V_a, the comparator changes state and this can be taken as the end of conversion (EOC) command.



The D/A output voltage becomes successively closer to the actual analog input voltage. It requires eight pulses to establish the accurate output regardless of the value of the analog input.

Correct Digital Representation	SAR Output Vd at Different Stages in the Conversion	Comparator Output
11010100	10000000	1 (Initial O/P)
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0

11. Explain Integrating Type of ADCs & Charge Balancing ADC

Integrating Type of ADCs

The integrating type of ADCs do not require a S/H circuit at the input.

If the input changes during conversion, the ADC output code will be proportional to the value of the input averaged over the integration period.

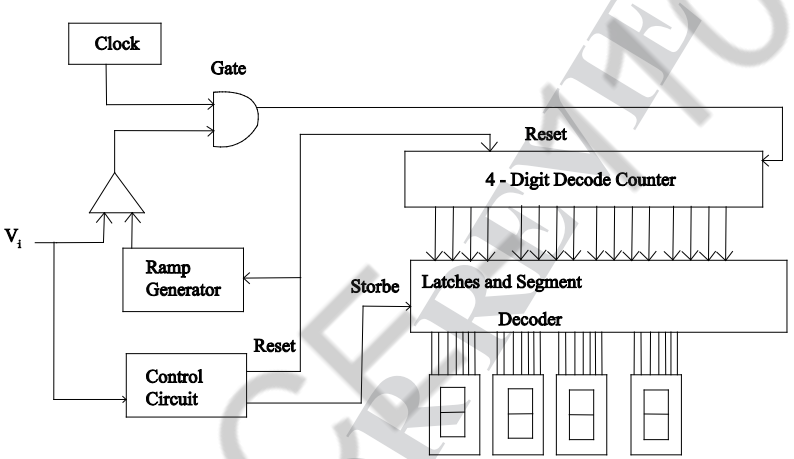
Charge Balancing ADC:

The principal of change balancing ADC is to first convert the input signal to a frequency using a voltage to frequency (V/F) converter. This frequency is then measured by a counter and converted to an output code proportional to the analog input.

The main advantage of these converters is that it is possible to transmit frequency even in noisy environment or in isolated form. The drawback of the change balancing ADC is eliminated by the dual slope conversion.

12. Explain with circuit the Single Slope ADC:

If short conversion time is not required, single slope or dual slope ADC can be used. This is based on comparing the unknown analog input with the reference voltage. Time required to reach the unknown analog input is proportional to the amplitude of analog input.



At the start, RESET signal is provided to the ramp generator and the counters.Analog input V_i is given to the non - inverting terminal of comparator. Since V_i is greater than –ve input, comparator output goes HIGH. HIGH output of comparator enables the AND gate which allows clock to reach to the counter and also this HIGH output starts the ramp. Ramp voltage goes positive until it exceeds the input voltage.

When it exceeds V_{in} comparator output goes low. This disables AND gate which inturn stop the clock to the counters. Latched data is then displayed using decoder and display device.

Eg:

Assume clock frequency = 1MHz

V_{in} = 2.000v

Ramp slope = 1v/ms

Since Vin = 2v, ramp will take 2ms to reach 2v.

No. of pulses reaches the counter during 2ms,

$$\frac{2\text{ms}}{(1/1\text{MHz})} = 2000$$

Inserting the decimal point at the proper point gives a reading of 2.000.

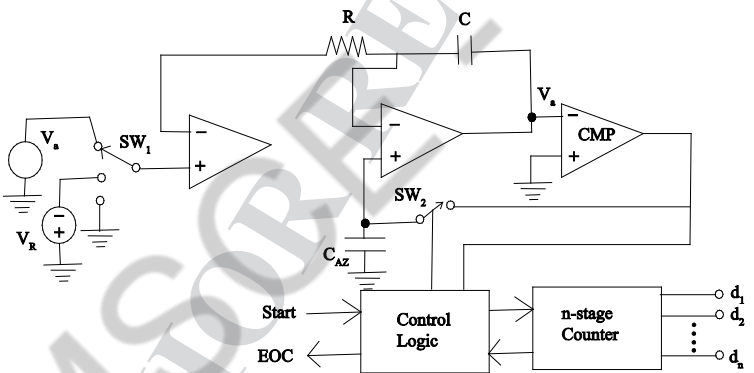
To get Binary output, Binary counters can be used.

Disadvantages:

Output voltage is a function of R and C. So, any change in R and C due to temperature introduce error.

Drift in clock frequency also causes error.

13. Explain the Dual – Slope ADC construction and working with necessary equations



The analog part of the circuit consists of a high input impedance buffer A_1, precision integrator A_2 and a voltage comparator. The converter first integrates the analog input sign a V_a for a fixed duration of 2^n clock periods. Then it integrates an internal reference voltage V_R of opposite polarity until the integrator output is zero.

The number N of clock cycles required to return the integrator to zero is proportional to the value of V_a averaged over the integration period. Hence N represents the desired output code.

Before the START command arrives, the switch SW_1 is connected to ground and SW_2 is closed. Any offset voltage present in the A_1, A_2, comparator loop after integration, appears across the capacitor C_{AZ} till the

threshold of the comparator is achieved.

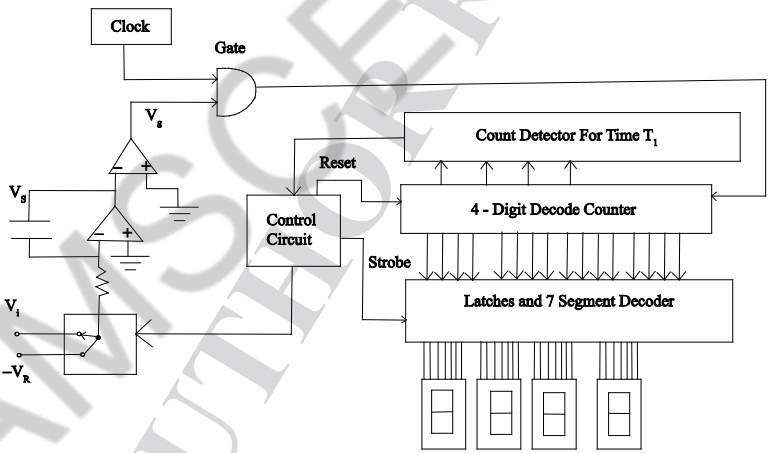
The capacitor C_{AZ} provides automatic compensation for the input – offset V_o Hages of all the three amplifies. When SW_2 opens, C_{AZ} acts as a memory to hold the voltage required to keep the offset nulled.

At the arrival of the start command at $t = t_1$, the control logic opens SW_2 and connects SW_1 to V_a and enables the counter starting from zero. The circuit uses an n – stage ripple counter and it resets to zero after counting 2^n pulses.

If the clock period is T, the integration takes place for a time $T_1 = 2^n \times T$ and the output it same.

Dual Slope Type A/D Converter:

In dual slope ADC, integrator generates two different ramps, one with the unknown analog input voltage V_i as the input and another with a known reference voltage $-V_c$ as the input. Hence, it is called dual slope A/D converter.



Assume that the 4 digit decode counter is initially reset to 0000. Ramp generator is switched between analog input voltage V_a and negative reference voltage $-V_{ref}$.

Switch is controlled by MSB of counter.

1. MSB = 0, Analog input will be connected to the ramp generator.

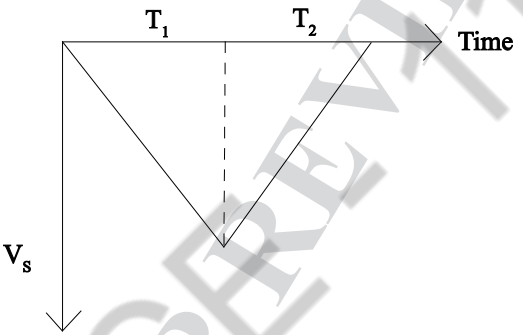
2. MSB = 1, $-V_{ref}$ will be connected to ramp generator.

Initially counter is reset to 0000. Thus MSB = 0 switches the V_a to ramp generator.

At the arrival of START command at $t = t_1$.

Control logic opens SW_2 and connect SW to V_a and enables the counter starting from zero.

The circuit uses n – stage ripple counter and therefore the counter resets to zero after counting 2^n pulses. Analog voltage V_a is integrated for a find number of 2^n counter of clock pulses after which the counter resets to zero.



$$-V_s = \frac{V_i}{Rc} \times T_1$$

$$V_s = -\left(\frac{-V_R}{Rc} \times T_2\right)$$

$$\frac{-V_i}{Rc} \times T_1 = \frac{V_R}{Rc} \times T_2$$

$$-V_i = V_R \times \frac{T_2}{T_1}$$

The output voltage of the integrator is given by

$$V_o = \frac{-1}{R_1C_1}\int_0^{t_1} V_i dt = \frac{-V_i}{R_1C_1} t_1$$

Then the analog switch will be connected to $-V_R$. This will cause the integrator output to ramp positive. When integrator output reaches zero, the comparator output goes low, which disables the clock AND gate.

This steps the clock pulses reaching the counter so that the counter will be stopped at a count corresponding to the number of clock pulses in time t_2.

Charging Voltage = Discharging Voltage

$$\frac{-V_i t_1}{R_1 C_1} = \frac{-V_R t_2}{R_1 C_1}$$

PROBLEMS IN D/A CONVERTERS

1. **An 8 bit DAC has an output voltage range of 0 – 2.55v. Define its resolution in 2 ways.**

Solution:

i) RESOLUTION = STEP SIZE = $\frac{V_{OFS}}{2^n - 1}$

$V_{OFS} = 2.55$

$n = 8$

$$R = \frac{2.55}{2^8 - 1} = 10mv \quad \Rightarrow \quad R = 10mv$$

ii) $R = 2^n = 2^8 = 256$

$R = 256$

2. **The digital input for a 4 bit DAC is 0110. Calculate its final output voltage.**

Solution:

For a given 4 bit DAC

$n = 4$

$V_{OFS} = 15$

$$R = \frac{V_{OFS}}{2^n - 1} = \frac{15}{2^4 - 1} = 1v/LSB$$

$R = 1v/LSB$

$V_o = R \times D$

$V_o = 1v/LSB \times 6 = 6v \quad \Rightarrow \quad V_o = 6v$

3. **An 8 bit DAC has resolution of 20 mv/LSB. Find V_{OFS} and no if input is $(10000000)_{21}$.**

Solution:

$R = 20$ mv/LSB

$n = 4$

$$R = \frac{V_{OFS}}{2^n - 1} \quad \Rightarrow \quad V_{OFS} = R\left(2^n - 1\right) = 20 \text{ mv/LSB}\left(2^8 - 1\right)$$

$V_{OFS} = 5.1v$

$D = (10000000)_2$

$= 128$

$V_o = R \times D = 20 \times 10^{-3} \times 128$

$V_o = 2.56$ v

4. **Find out step size and analog output for 4 – bit R – 2R ladder DAC when input is 1000 and 1111. Assume $V_{ref} = +5v$.**

Solution:

$n = 4$

$V_{OFS} = 5v$

$$\text{Resolution} = \frac{V_{OFS}}{2^n - 1} = \frac{5}{2^4 - 1} = 0.33v/LSB$$

$R = 0.33v/LSB$

$V_o = R \times D$

For input = 1000 $\quad \Rightarrow \quad D = 8$

$V_o = 0.33 \times 8$

$V_o = 2.6667v$

For input = 1111 $\quad \Rightarrow \quad D = 9$

$V_o = 0.33 \times 15$

$V_o = 5v$

5. **A 12 – bit DAC has a step size 8mv. Determine V_{OFS} and %resolution. Also find V_o for input 010101101101?**

Solution:

$$R = \frac{V_{OFS}}{2^n - 1} \Rightarrow 8 \times 10^{-3} = \frac{V_{OFS}}{2^{12} - 1} \Rightarrow V_{OFS} = 32.76v$$

$$\%\text{Resolution} = \frac{8mv}{32.76v} \times 100$$

For input = 010101101101

$D = (1389)_{10}$

$V_o = 8mv \times 1389 \Rightarrow V_o = 11.112v$

6. **A system uses a 12 – bit word to represent the input signal. If the maximum peak – to – peak voltage at the output is set to 4v. Find the resolution of the system and the dynamic range.**

Solution:

$$\text{Resolution} = \frac{4v}{4096 - 1} = 976\mu v$$

$$\text{Dynamic Range} = \frac{4v}{976\mu v} = 4096$$

$20 \log(4096) = 72dB$

Dynamic range gives the ratio of largest value to the smallest value which can be converted.

7. **The basic step of a 9 – bit DAC is 10.3mv. If 000000000 = 0v what is the output for an input of 101101111.**

Solution:

$V_o = \text{Resolution} \times D$

$V_o = 10.3 \times 10^{-3} \times 367$

$V_o = 3.7801v$

For 101101111

$D = 367$

8. **If the maximum output voltage of a 7 – bit D/A is 25.4v. What is the smallest change in the output as the binary count increase.**

Solution:

$$\text{Resolution} = \frac{\text{OFS}}{2^n - 1} = \frac{25.4}{2^7 - 1} = \frac{25.4}{128 \quad 1} = 0.2\text{v}$$

9. **How many bits required to design a DAC, that can have resolution of 5mv?The ladder has +8v full scale.**

Solution:

$$\text{Resolution} = \frac{V_{OFS}}{2^n - 1}$$

$$2^n = \frac{V_{OFS}}{\text{RESOLUTION}} + 1 = \frac{8}{5 \times 10^{-3}} + 1$$

$2^n = 1601$

Take log on both sides

$$n \log 2 = \log 1601 \quad \Rightarrow \quad n = \frac{\log 1601}{\log 2}$$

$n = 10.644$

$n \simeq 11$

10. **Find the resolution of 12 – bit DAC.**

Solution:

Resolution $= 2^n = 2^{12} = 4096$

11. **Calculate the values of LSB, MSB and full scale output for an 8 bit DAC for 0 – 10v range.**

Solution:

$$V_o = V_{FS}\left[\underbrace{d_1 2^{-1}}_{\text{MSB}} + d_2 2^{-2} + \ldots\ldots \underbrace{d_8 2^{-8}}_{\text{LSB}}\right]$$

12. **How many levels are possible in a 2 bit DAC. What is its resolution if the output range is 0 – 3v?**

Solution:

No. of Levels $= 2^n = 2^2 = 4$

$$\text{Resolution} = \frac{V_{OFS}}{2^n - 1} = \frac{3}{2^2 - 1} = \frac{3}{3} = 1$$

$$\%\text{Resolution} = \frac{1}{3} \times 100 = 33.33\%$$

13. A 5 bit D/A converter is available. Assume that '00000' corresponds to an output of +10v and that D/A converter is connected for −0.1v per increment, what output voltage will be produced for 11111?

Solution:

Step Size $= -0.1$v

For 00000, output $= +10$v

For 00000, analog equivalent $= 0$

For 11111, analog equivalent $= 31$

$31 \times (-0.1) = -3.1$

$10 - 3.1 = 6.9$

14. If a 10 bit DAC spans a range of 0 – 10v and is always within 1mv of its ideal output. What is its linearity as a percentage of full scale range?

Solution:

Linearity is defined as the deviation of actual output from ideal output expressed as

$$\text{Linearity} = \frac{\epsilon}{\Delta}$$

$\epsilon = 1$mv

$$\Delta = \text{Step Size} = \frac{V_{OFS}}{2^n - 1} = \frac{10}{1024 - 1} = \frac{10}{1023}$$

$$\text{Linearity} = \frac{1 \times 10^{-3}}{\frac{10}{1023}}$$

$$= 0.102$$

A/D CONVERTERS

15. Dual slope ADC uses a 16 bit counter and a 4MH clock rate. The maximum input voltage is +10v. The maximum integrator output voltage should be −8v when the counter has cycled through 2^n counts. The capacitor used in the integrator is 0.1μF. Find the value of the resistor R of the integrator.

Solution:

$n = 16$

$F_c = 4MHz$

$V_{iFS} = 10v$

$$V_s = -\frac{1}{Rc} V_i T_1$$

$$-8 = -\frac{1}{R \times 0.1 \times 10^{-6}} \times 10 \times \frac{2^{16}}{4 \times 10^6}$$

$R = 205K\Omega$

1 T_1 4×10^6 2^n

1 T_1 4×10^6 2^n

$T_1 \times 4 \times 10^6 = 2^n$

$$T_1 = \frac{2^{16}}{4 \times 10^6}$$

16. If analog signal V_a is +4.129v in the previous example. Find the equivalent digital number.

Solution:

$$N = 2^n \left(V_a / V_R \right) \Rightarrow 2^{16} \left(\frac{4.126}{8} \right) = 33825$$

Binary equivalent = 1000010000100001

17. The analog input signal ranges for −5 to +8v in a 9 bit ADC.

a) How many quantization levels are available with this A/D converter.

b) What is the resolution in volt per increment.

c) What binary number will be produced when the analog input is zero volt.

Solution:

No. of quantization level $= 2^n = 2^9 = 512$

$$\text{Resolution} = \frac{V_{iFS}}{2^n - 1} = \frac{8-(-5)}{512-1} = 0.0254$$

When analog input is 0,

$$\text{analog output} = (0 - (-5)) \times 0.0254$$

$$= 0.127$$

18. What is the conversion time of a 10-bit successive approximation A/D converter if its input clock is 5 MHz.

Solution:

$Tc = T(n + 1)$

$$T_c = \frac{1}{5\times10^6}(10+1) \quad \Rightarrow \quad T = 22\mu s$$

19. A dual slope ADC uses a 18 bit counter with a 5MHz clock. The maximum input voltage is +12v and maximum integrator output voltage at 2^N count is -10v. If R = 100KΩ. Find the size of the capacitor.

Solution:

$$V_s = -\frac{1}{Rc}V_iT$$

$$-10 = -\frac{1}{100}\times12\times\frac{2N}{10^6}$$

1 T 5×10^6 2^N

$T \times 5 \times 10^6 = 2^N$

$$T = \frac{2^N}{5\times10^6}$$

n = 0.629 μFS

20. The dual slope ADC of previous has an input voltage of +5.237v. Determine the digital number in binary which represent the count in the register.

Solution:

$$N = 2^n\left(\frac{V_a}{V_R}\right)$$

$$N = 2^{18}\left(\frac{5.237}{10}\right) \quad \Longrightarrow \quad N = 137284.8$$
$$N = 137285$$

Binary equivalent = 101000100001100001

21. An 8 bit ADC outputs all 1's when V_i = 5.1v. Find it's a) Resolution b) digital output when V_i = 1.281.

Solution:

a) Resolution $= 2^n = 2^8 = 256$

$$\text{Resolution} = \frac{V_{iFS}}{2^n - 1} = \frac{5.1}{2^8 - 1} = 20\text{mv/LSB}$$

Thus to change output by 1LSB we have to change input by 20mv.

b) For $V_i = 1.28$v

$$D = \frac{1.28}{20\text{mv/LSB}} \quad \Rightarrow \quad D = 64 \text{ LSB}$$

The binary equivalent of 84 is $0100\ \ 0000_2$

22. Calculate quantization error for 12 bit ADC with full scale input voltage 4.095V.

Solution:

$$Q_E = \frac{4.095}{\left(2^{12} - 1\right)2} \quad \Rightarrow \quad Q_E = 0.5\text{mv}$$

23. for a particular dual slope ADC, t_1 is 83.33ms and the V_{ref} = 100mv. Calculate t_2 if V_i is 100mv.

Solution:

$$t_2 = \left(\frac{V_i}{V_R}\right)t_1$$

$$= \left(\frac{100}{100}\right)83.33\text{ms} \quad \Rightarrow \quad t_2 = 83.33\text{ms}$$

24. Find the digital output of an ADC having t_1 as 83.33ms and V_R as 100mv for an input voltage of +100mv. The clock frequency is 12KHz.

Solution:

Digital output $= F_c \; t_2$

$$= (\text{counts/sec}) \;\; t_1\left(\frac{V_i}{V_R}\right)$$

$$=12\times10^3\times83.33\times10^{-3}\times\frac{100}{100}$$

$$= \text{counts}$$

$$=\frac{-R_2}{R_1}\left(V_2+\frac{R_1}{R}(V_2-V_1)\right)+\left(1+\frac{R_2}{R_1}\right)\left(\frac{R_2}{R_1+R_2}\right)\left(V_1-\left(\frac{R_1}{R}\right)(V_2-V_1)\right)$$

$$=\frac{-R_2}{R_1}V_2\frac{-R_2R_1}{RR_2}(V_2-V_1)+\left(\frac{R_1+R_2}{R_1}\right)\left(\frac{R_2}{R_1+R_2}\right)\left(V_1-\left(\frac{R_1}{R}\right)(V_2-V_1)\right)$$

$$=\frac{-R_2}{R_1}V_2\frac{-R_2R_1}{RR_1}(V_2-V_1)+\left(\frac{R_2}{R_1}\right)\left(V_1-\left(\frac{R_1}{R}\right)(V_2-V_1)\right)$$

$$=\frac{-R_2}{R_1}V_2\frac{R_2R'}{RR'}(V_2-V_1)+\frac{R_2}{R_1}V_1-\left(\frac{R_2R'}{RR'}\right)(V_2-V_1)$$

$$=\frac{R_2R'}{RR'}(V_2-V_1)\left(\frac{R_2R'}{RR'}\right)(V_2-V_1)$$

Ans: Res: 1, 2, 3, 4, 5, 6, 9, 13, 14, 17, 21, 22, 23, 24, 25, 27, 30, 32, 33, 34, 35, 36

14. Design a second order Butterworth LPF having upper cutoff frequency 1KHz.

Solution:

Given: Fn = 1KHz =, Let C = 0.1 μF, $\propto = 1.414$

$$\frac{1}{2\pi Rc}=1\times10^3 \quad \Rightarrow \quad R=\frac{1}{2\times3.14\times1\times10^3\times0.1\times10^{-6}}$$

$$R = 1.6K\Omega$$

$\propto = 3 - A_o \implies A_o = 3 - \propto = 3 - 1.414$

$A_o = 1.586$

The transfer function

$$H(s) = \frac{A_o}{S_n^{\,2} + \alpha S_n + 1}$$

$$H(s) = \frac{1.586}{S_n^{\,2} + 1.414 S_n + 1}$$

$$A_o = 1 + \frac{R_F}{R_i} \Rightarrow \frac{R_F}{R_i} = A_o - 1 \Rightarrow \frac{R_F}{R_i} = 0.586$$

Let $R_i = 10K\Omega \implies R_F = 5.86K\Omega$

UNIT - 5

WAVEFORM GENERATORS AND SPECIAL FUNCTION ICs

PART-A

1. **Mention some applications of 555 timer (DEC 2009)**
   - Oscillator
   - pulse generator
   - ramp and square wave generator
   - mono-shot multivibrator
   - burglar alarm
   - traffic light control.

2. **List the applications of 555 timer in monostable mode of operation:**
   - missing pulse detector
   - Linear ramp generator
   - Frequency divider
   - Pulse width modulation.

3. **List the applications of 555 timer in Astable mode of operation: (MAY/JUNE 2010)**
   - FSK generator
   - Pulse-position modulator

4. **What is a voltage regulator? (MAY 2010)**
   A voltage regulator is an electronic circuit that provides a stable dc voltage independent of the load current, temperature, and ac line voltage variations.

5. **Give the classification of voltage regulators: (MAY 2010)**
   *Series / Linear regulators
   *Switching regulators.

6. What is a linear voltage regulator?

Series or linear regulator uses a power transistor connected in series between the unregulated dc input and the load and it conducts in the linear region .The output voltage is controlled by the continous voltage drop taking place across the series pass transistor.

7. What is a switching regulator?

Switching regulators are those which operate the power transistor as a high frequency on/off switch, so that the power transistor does not conduct current continously.This gives improved efficiency over series regulators.

8. What are the advantages of IC voltage regulators?

- low cost
- high reliability
- reduction in size
- excellent performance

9. Give some examples of monolithic IC voltage regulators:

78XX series fixed output, positive voltage regulators

79XX series fixed output, negative voltage regulators

723 general purpose regulator.

10. What is the purpose of having input and output capacitors in three terminal ICregulators?

A capacitor connected between the input terminal and ground cancels the inductive effects due to long distribution leads. The output capacitor improves the transient response.

11. Define line regulation.

Line regulation is defined as the percentage change in the output voltage for a change in the input voltage.It is expressed in millivolts or as a percentage of the output voltage.

12. Define load regulation.

Load regulation is defined as the change in output voltage for a change in load current. It is expressed in millivolts or as a percentage of the output voltage.

13. What is meant by current limiting?

Current limiting refers to the ability of a regulator to prevent the load current from increasing above a preset value.

14. Give the drawbacks of linear regulators:

- The input step down transformer is bulky and expensive because of low line frequency.
- Because of low line frequency,large values of filter capacitors are required to decrease the ripple.
- Efficiency is reduced due to the continous power dissipation by the transistor as it operates in the linear region

15. What is the advantage of monolithic switching regulators? (MAY 2010)

- Greater efficiency is achieved as the power transistor is made to operate as low impedance switch.Power transmitted across the transistor is in discrete pulses rather than as a steady current flow.
- By using suitable switching loss reduction technique, the switching frequency
- Can be increased so as to reduce the size and weight of the inductors and capacitors

16. What is an opto-coupler IC? Give examples. (MAY 2010)

Opto-coupler IC is a combined package of a photo-emitting device and a photo- sensing device.Examples for opto-coupler circuit :

LED and a photo diode, LED and photo transistor, LED and Darlington.

Examples for opto-coupler IC : MCT 2F , MCT 2E .

17. Mention the advantages of opto-couplers:

- Better isolation between the two stages.
- Impedance problem between the stages is eliminated. *Wide frequency response.
- Easily interfaced with digital circuit.
- Compact and light weight.
- Problems such as noise, transients, contact bounce,.. are eliminated.

18. What is an isolation amplifier? (MAY/JUNE 2010)

An isolation amplifier is an amplifier that offers electrical isolation between its input and output terminals.

19. What is the need for a tuned amplifier? (MAY 2009)

In radio or TV receivers , it is necessary to select a particular channel among all other available channels.Hence some sort of frequency selective circuit is needed that will allow us to amplify the frequency band required and reject all the other unwanted signals and this function is provided by a tuned amplifier.

20. Give the classification of tuned amplifier:

(i) Small signal tuned amplifier

- Single tuned
- Double tuned
- Stagger tuned

(ii) Large signal tuned amplifier.

21. Write the frequency of oscillation (f0) equation for triangular wave generator. (MAY 2010)

f0=R3/4R1C1R2

22. How frequency to voltage converted on OP-AMPS. (MAY 2010)

A Frequency to voltage converter produces an output voltage, whose amplitude is a function of frequency of the input signal. The input signal may be a sine- wave, a square wave or a pulse train. The F/V converter is essentially an FM detector or discriminator.

23. What is video amplifier? (MAY/JUNE 2010)

The video or wideband amplifiers are designed to provide a relatively flat gain versus frequency response characteristics for the range of frequencies required to transmit video information.

24. Define Multivibrators. Mention its types. (MAY/JUNE 2010)

Multivibrators are regenerative circuits, Which are mainly used in timing applications. Based on their operational characteristics they can be classified into

- Astable Multivibrators
- Monostable Multivibrators
- Bistable Multivibrators

25. Define Astable Multivibrators.

The astable Multivibrators toggles between one state and the other without the influence of any other external control signal. It is also called as free running multivibrator.

26. Define Monostable Multivibrators

The monostable multivibrator or one –shot requires an external signal called a trigger to force the circuitinto a quasi stable state for a particular time or delay.

27. What is audio amplifier?

The amplifier receives an input from signal source or from a transducer and gives out an amplified signal to the output device is called an audio amplifier.

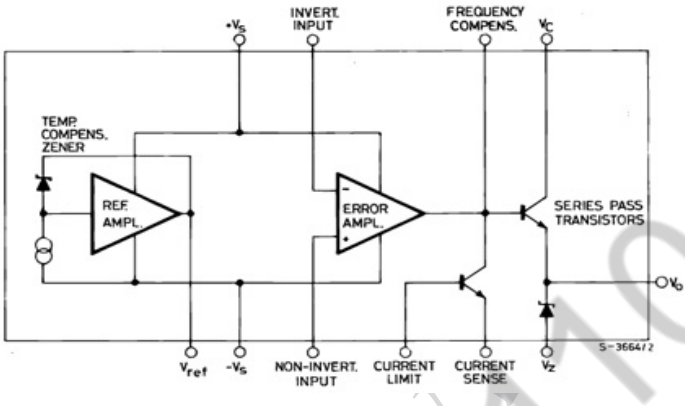
28. State the two conditions for oscilation. (April/May 2015)

1. Total phase shift should be zero or 360 degree.

2. The product of gain and feedback factor should be unity ($A\beta=1$)

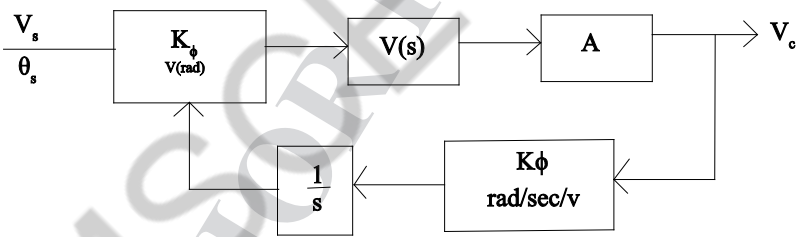
29. Draw the functional block diagram of 723 regulator.

(April/May 2015)



PART-B

1. Explain the Close Loop Analysis of PLL



Lø → conversion gain of phase detector

F(s) → loop filter transfer function

A → gain of the amplifier

Kθ → voltage to frequency transfer co-off of VCO

$$w_o(t) = \frac{d_{\theta_o}}{dt}$$

$$\theta_o(t) = \theta_o|_{t=0} + \int_0^t w_o(t)\, dt$$

Thus integration is represented by $\frac{1}{s}$ block.

When $V_c = 0$, VLC frequency is called as free running frequency.

Relation b/w VLC output frequency w_o and V_c is given by

$$w_o(t) = w_c + K_o V_c(t)$$

$$\frac{V_c}{\theta_s} = \frac{K\phi\, F(s) A}{1 + \frac{K\theta\, K\phi\, F(s) A}{s}} = \frac{s\, K\phi\, F(s) A}{s + K\theta\, K\phi\, F(s) A}$$

$$\theta_s = \frac{1}{s} w_s$$

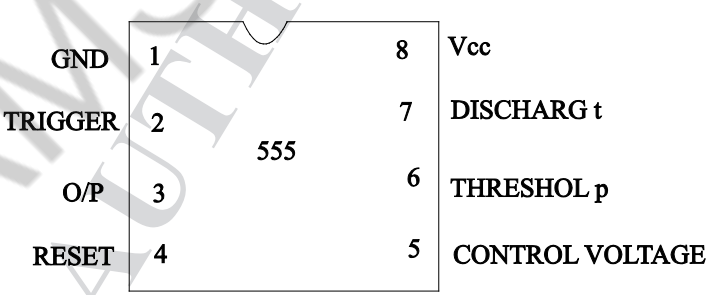
$$\frac{1}{s\,\theta_s} = \frac{1}{w_s} \qquad \text{and} \quad \text{if } F(s) = 1$$

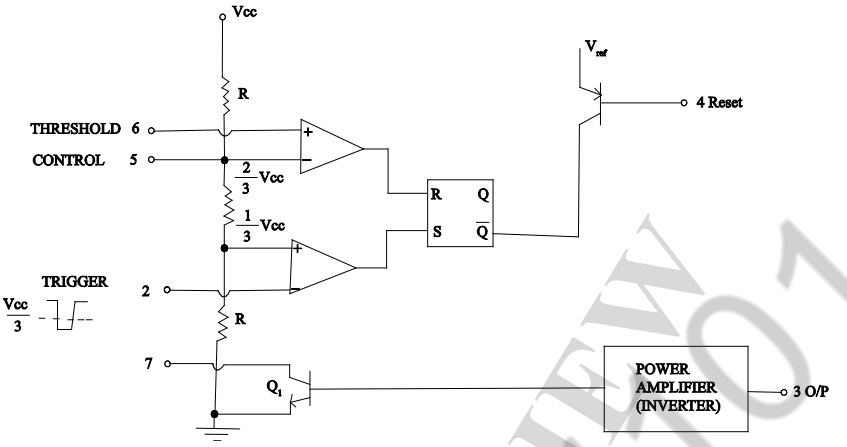
$$\frac{V_c}{w_s} = \frac{K\phi\, A}{s + K\phi\, K\theta\, A}$$

$$= \left(\frac{K_L}{s + K_L}\right)\frac{1}{K\theta}$$

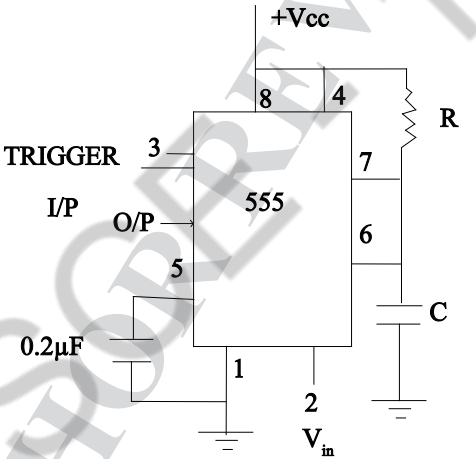
Where $K_L = K\phi\, K\theta\, A$ → Loop bandwidth

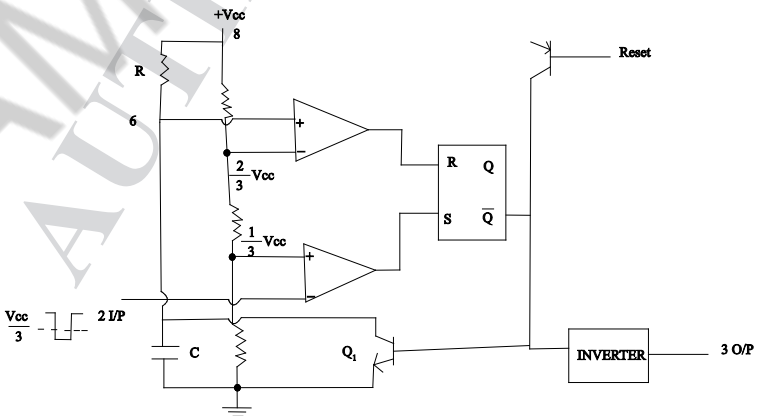
2. Draw the 555 Timer IC and its internal circuit:





3. Explain the Monostable Multivibrator Using 555 Timer:



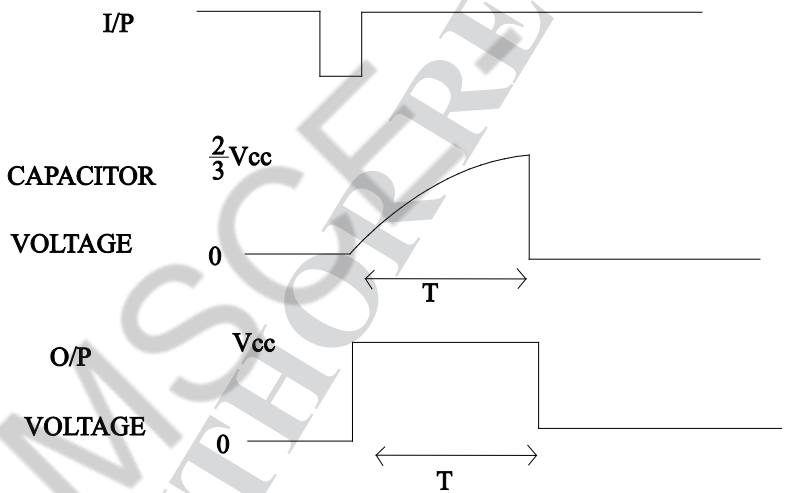


Under RESET condition, $Q = 0$, $\overline{Q} = 1$. $\overline{Q}$ is fiven to transistor Q_1 as will as to the inverter. Thus output $V_o = 0$. Since Base voltage is positive, Q_1 will act as a switch. So the capacitor voltage will get damped to 0v. $V_c =$ 0v. Now, if the negative triggering signal applied to the lower comparator and if that value goes below $\frac{1}{3}$ Vcc, lower comparator will trigger.

Thus $S = 1$, $Q = 1$, $\overline{Q} = 1$. This $\overline{Q}$ value will make the output $V_o = 1$ and also Q_1 will OFF. So the capacitor will charge towards +Vcc when the capacitor voltage V $-$Vcc upper comparator will

trigger. This will RESET the flip flap.

$Q = 1$, $\overline{Q} = 1$, $V_o = 0$



$$V_c(t) = Vcc\left(1 - e^{-t/Rc}\right)$$

At $t = T$, $V_c(t) = \frac{2}{3}Vcc$

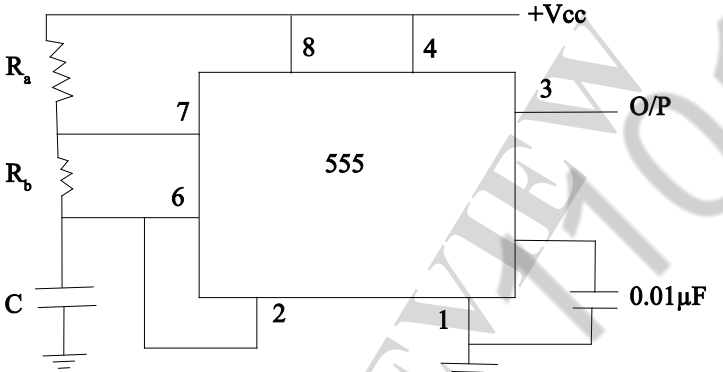
$$\frac{2}{3}Vcc = Vcc\left(1 - e^{-T/Rc}\right)$$

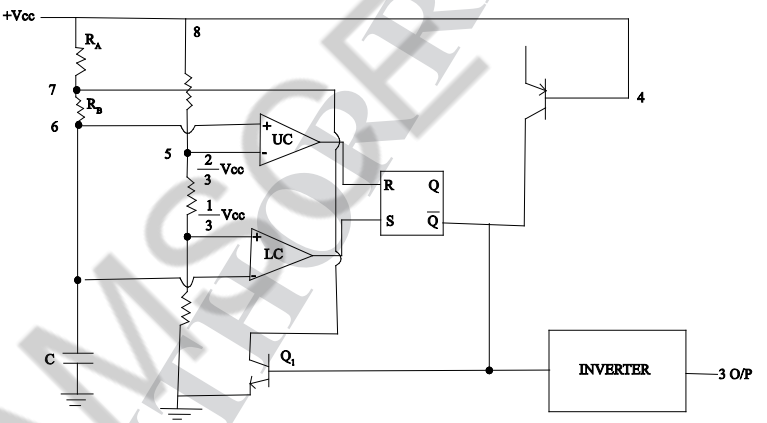
$$+\frac{1}{3} = +e^{-T/Rc}$$

$$T = Rc \text{ in}\left(\frac{1}{3}\right)$$

$T = 1.1Rc$

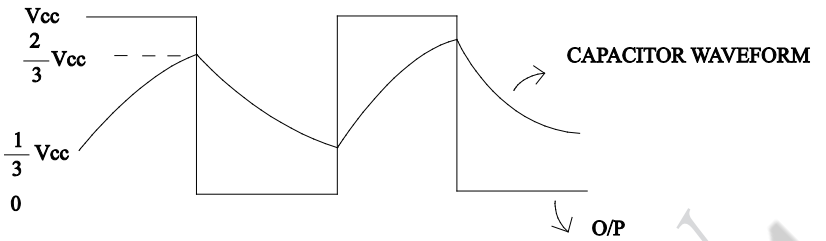
4. Explain AStable Multivibrator Using 555 Timer:





Assume $Q = 1$, $\overline{Q} = 0$. Thus $V_o = +Vcc$. For this assumption is $\overline{Q} = 0$, Q_1 will turn OFF. So, the capacitor C will charge through R_A and R_B. When the capacitor voltage becomes equal to reference value, comparator will reset the flip flop. $Q = 1$, $\overline{Q} = 1$, $V_o = 0$v. ($\overline{Q} = 1$) value will turn ON the Q_1. So the capacitor will discharge through R_B.

Again when the amplitude of discharging waveform becomes equal to $\frac{1}{3}$Vcc, lower comparator will trigger and it will set the F/F. Thus the above 2 processes will repeat cyclically. Thus the square wave can be generated.



$$V_c = Vcc\left(1 - e^{-t/Rc}\right)$$

Let t_1 be the time taken by the capacitor to charge from 0 to $\frac{2}{3}Vcc$.

At $t = t_1$, $V_c = \frac{2}{3}Vcc$

$$\frac{2}{3}Vcc = Vcc\left(1 - e^{-t_1/Rc}\right)$$

$t_1 = 1.09Rc$

Let t_2 be the time taken by the capacitor to charge from 0 to $\frac{1}{3}Vcc$

At $t = t_2$, $V_c = \frac{1}{3}Vcc$

$$\frac{1}{3}Vcc = Vcc\left(1 - e^{-t_2/Rc}\right)$$

$t_2 = 0.405Rc$

Time taken by the capacitor to change from $\frac{1}{3}Vcc$ to $\frac{2}{3}Vcc$ is $t_1 - t_2$.

$t_{HIGH} = t_1 - t_2$

$= 1.09Rc - 0.405Rc$

$t_{HIGH} = 0.69Rc$

$t_{HIGH} = 0.69(R_A + R_B)C$

$t_{LOW} = 0.69Rc$

$t_{LOW} = 0.69\ R_B\ C$

$T = t_{HIGH} + t_{LOW} = 0.69(R_A + R_B)C + 0.69\ R_B\ C$

$T = 0.69(R_A + 2R_B)C$

$$f = \frac{1}{T} = \frac{1}{0.69(R_A + 2R_B)C}$$

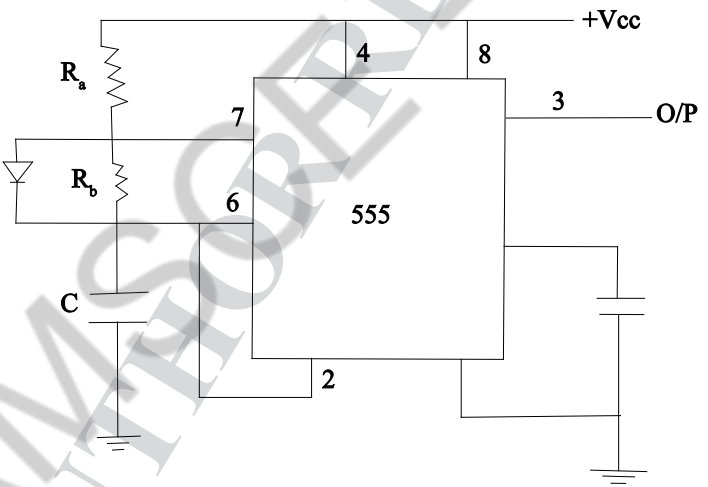
$$f = \frac{1.45}{(R_A + 2R_B)C}$$

$$D = \frac{t_{LOW}}{T} = \frac{0.69R_BC}{0.69(R_A + 2R_B)C}$$

$$D = \frac{R_B}{R_A + 2R_B}$$

Since t_{LOW}, t_{HIGH} are unequal, only asymmetrical waveform can be generated by this circuit.

To get symmetrical waveform. Diode have to be connected in parallel with R_B.



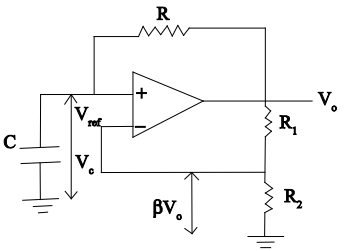
For this, $t_{HIGH} = 0.69Rc$

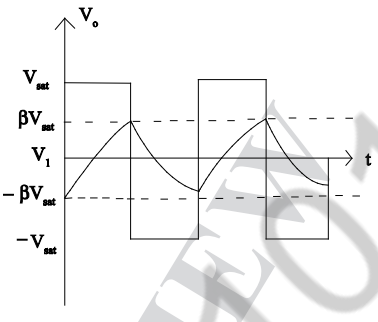
$t_{LOW} = 0.69\ R_B\ C$

$$f = \frac{1}{T} = \frac{1.45}{(R_A + R_B)C}$$

$$D = \frac{R_B}{R_A + R_B}$$

5. Explain the Astable Multivibrator [Wave Oscillator] using OP-AMP





Fraction of the output is β is feedback to the '+' terminal of an op-amp.

$$\beta = \frac{R_2}{R_1 + R_2}$$

$$\therefore \quad V_{ref} = \beta V_o = \pm \beta V_{sat}$$

output is also feedback of '−' terminal after integrating by means of a low pass Rc circuit.

Whenever input at '−' terminal exceeds V_{ref}, switching takes place, results in square wave output. In astable multivibrator, both stable are quasi stable.

Consider at some time t, $V_o = +V_{sat}$

$$\therefore \quad V_{ref} = +\beta V_{sat}$$

Capacitor will start to charge towards $+\beta V_{sat}$.

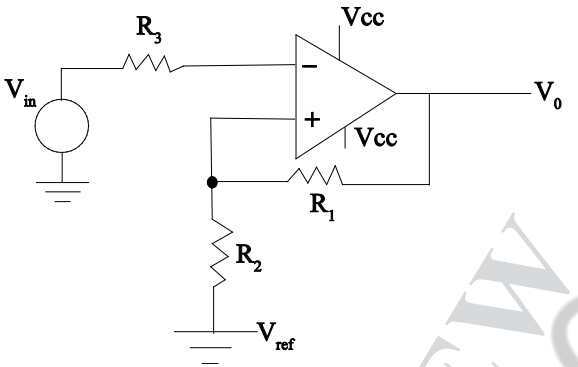
When it reaches $+\beta V_{sat}$, switching takes place so the output will be driven to $-\beta V_{sat}$.

Now $V_{ref} = -\beta V_{sat}$

So the capacitor will now start to charge towards $-\beta V_{sat}$.

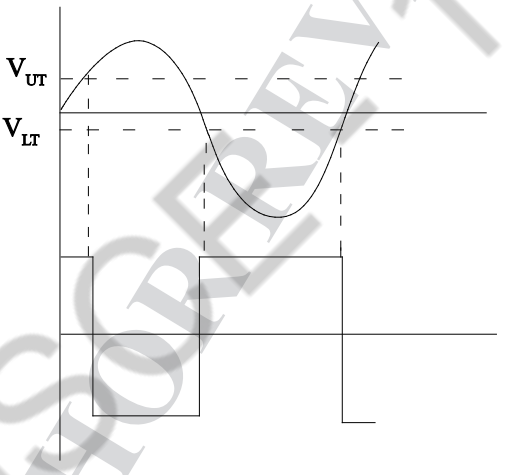
If it reaches $-\beta V_{sat}$, again switching will takes place.

The cycle repeats.



$V_{in} > V_{ref}$, $V_o = -V_{sat}$

$V_{in} < V_{ref}$, $V_o = +V_{sat}$



Voltage across caoacitor

$$V_c(t) = V_f + (V_i - V_f)e^{-t/Rc}$$

Final value $V_f = +V_{sat}$

Initial value $V_i = -\beta V_{sat}$

$$V_c(t) = V_{sat} + (-\beta V_{sat} - V_{sat})e^{-t/Rc}$$

$$V_c(t) = V_{sat} - V_{sat}(1+\beta)e^{-t/Rc}$$

At $t = T_1$,

$$V_c(T_1) = \beta V_{sat} = V_{sat} - V_{sat}(1+\beta)e^{-T_1/Rc}$$

$$T_1 = Rc \text{ in}\left(\frac{1+\beta}{1-\beta}\right)$$

Total Time Period = $2T_1$

$$T = 2Rc \text{ in}\left(\frac{1+\beta}{1-\beta}\right)$$

If $R_1 = R_2 \implies B = 0.5$

$T = 2Rc$

$$f_o = \frac{1}{2Rc}$$

Peak to Peak = $2\ V_{sat}$

Peak to peak value can be varied by varying the power supply voltage.

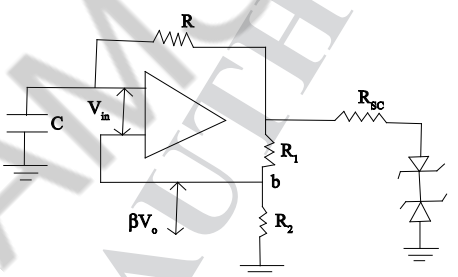
One of the technique is using back to back zever diodes

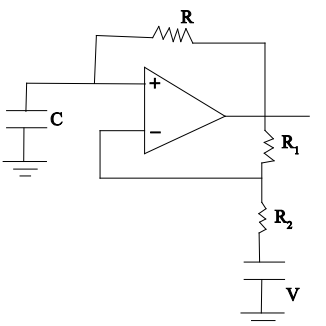
V_o (Peak to Peak) = $2(V_Z + V_D)$

If asymmetric square wave is desired, Zever diode with different break down voltages are used.

$V_{01} = V_{Z1} + V_D$; $V_{02} = V_{Z2} + V_D$

$$T_1 = Rc \text{ in}\left(\frac{1+\beta V_{02}/V_{01}}{1-\beta}\right)$$





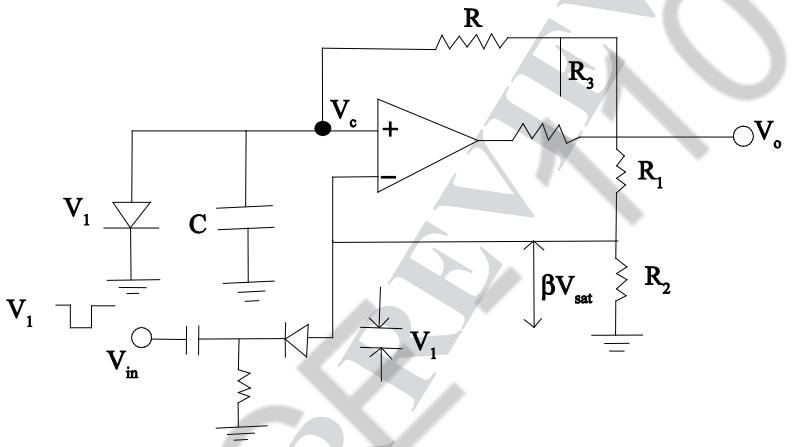
$V_{01} = \beta\ V_{sat} + V$

$V_{02} = \beta\ V_{sat} + V$

6. Explain Monostable Multivibrator using OP-AMP

Monostable multivibrator is also called as or shot multivibrator. The circuit produces a signal pulse of specs duration in response to each external triggers. For such a circuit only one stable state exist.

When an external trigger pulse applied, output changes its state. The new state is called quase stable state. The circuit remains in this stable for a fixed internal of time. After this, the circuit will again return back to the orig stable state.



Diode D_1 is a clamping diode which damped the capacitor voltage to 0.7v when output $= +V_{sat}$.

'$-$'ve triggering pulse applied to '$+$' input terminal through D_1.

Diode D_2 is used to black the positive noise spikes that may be present at the differentiated trigger input. Assume $V_o = +V_{sat}$ ie in stable state. Diode D_1 conducts, V_c will be damped to 0.7v.

Voltage at '$+$' terminal is $\beta V_o = +\beta V_{sat}$

Now negative trigger of amplitude V_1 is applied to '$+$' terminal.

Thus effective voltage at '$+$' terminal $= \{+\beta V_{sat} + (-V_1)\} < 0.7V$

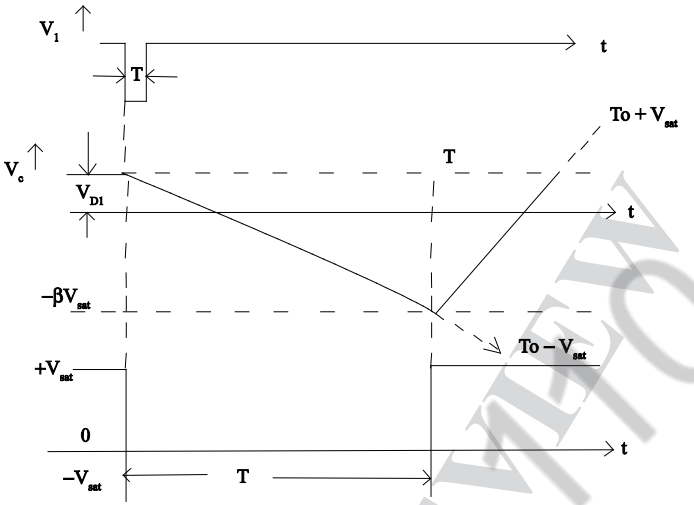
So the output of op-amp changes from $+V_{sat}$ to $-V_{sat}$.

Diode is now reverse biased capacitor now starts charging exponentially to $-V_{sat}$ through the resistor R.

Time constant of this charging $C = Rc$

Voltage at the '$+$' terminal is $-\beta V_{sat}$.

When the V_c reaches $-\beta V_{sat}$, again the output will switch back to $+V_{sat}$.



Expression For Pulse Width T

V_i = Initial Voltage

V_f = Final Voltage for low pass Rc circuit

$$V_c = V_f + (V_i - V_f)e^{-t/Rc}$$

$$V_f = -V_{sat}; \quad V_i = V_{D1}$$

$$V_c = -V_{sat} + (V_{D1} + V_{sat})e^{-t/Rc} \qquad 1$$

At $t = T$

$$V_c = -\beta V_{sat} \qquad 2$$

Equate 1 & 2

$$-\beta V_{sat} = -V_{sat} + (V_{D1} + V_{sat})e^{-T/Rc}$$

$$(V_{D1} + V_{sat})e^{-T/Rc} = V_{sat}(1-\beta)$$

$$e^{-T/Rc} = \frac{V_{sat}(1-\beta)}{V_{D1} + V_{sat}}$$

$$T = Rc \ \text{in}\left[\frac{1 + \frac{V_{D1}}{V_{sat}}}{1-\beta}\right]$$

If $R_1 = R_2$; $\beta = 0.5$

Also if $V_{sat} >> V_{D1}$

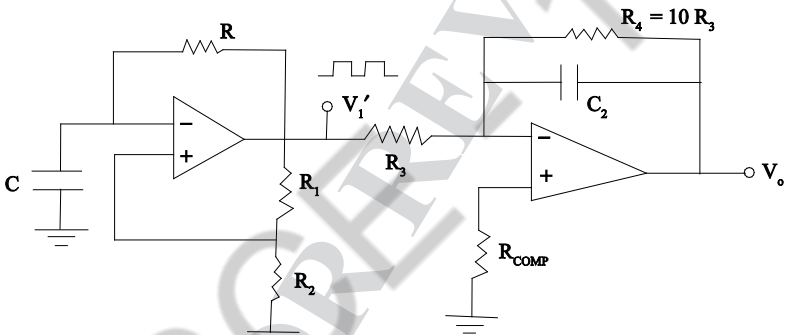
$T = 0.69\ RC$

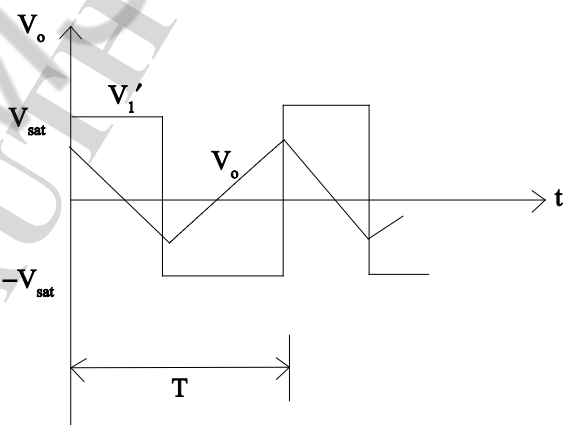
For monostable operation, $T_P < T$

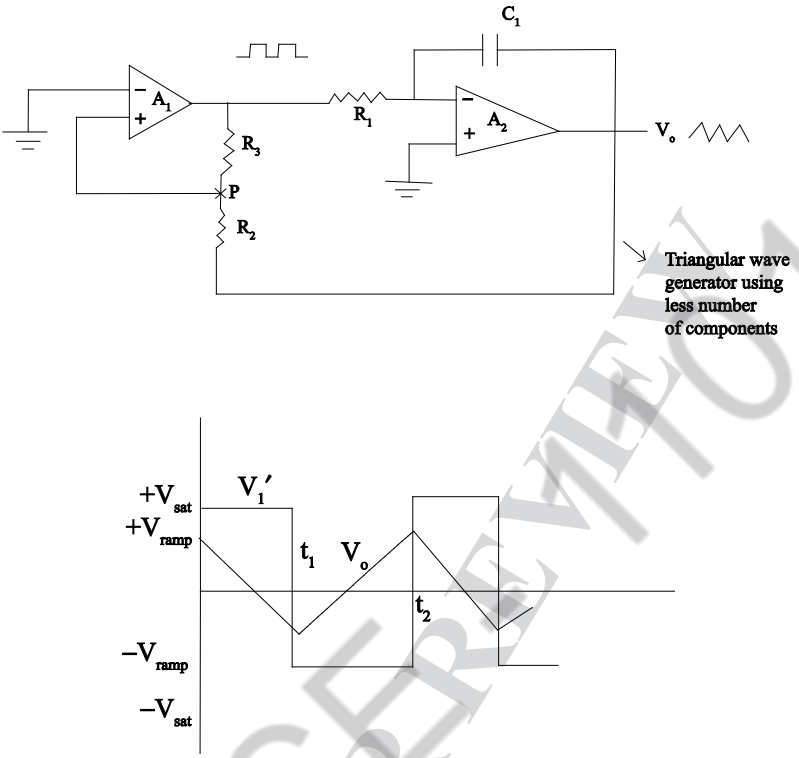
7. Explain the Triangular Wave Generator:

Triangular wave can be obtained by integrating a square wave. Frequency will be same for both triangular wave and square wave. Amplitude of the square wave is constant at ± Vsat, the amplitude of triangular wave ↓ with ↑ frequency and vice versa. This is because the reactance of capacitor ↓ at high frequency & ↑ at low freq.

R_4 = to avoid saturation problem at low frequency.







Output of comparator A_1 is square wave of $+V_{sat}$ and is applied to the (−) terminal of produces triangular wave. This triangular wave is fed back as input to A through voltage divider R_2R_3.

Consider output of $A_1 = +V_{sat}$ Thus The output of integrator A_2 will be rega going ramp.

One end of voltage divider is at $+V_{sat}$ other and is at −ve going ramp. At t = t_1, when negative going ramp ate $-V_{ramp}$, voltage at point P becomes be than 0v. This switches the output from $+V_{sat}$ to $-V_{sat}$

When the output of A_1 is $-V_{sat}$, output of A_2 ↑ in the +ve direction. At t = t_2, voltage at point P becomes just above 0v, thereby switching the output from $-V_{sat}$ to $+V_{sat}$. The cycle repeats and generates a triangular wave. Amplitude of triangular wave depends on Rc value of integrator A_2 and V_o of A_1.

Amplitude and Frequency Calculation:

When comparator output is $+V_{sat}$, effective voltage at point P is

$$-V_{ramp}+\frac{R_2}{R_2+R_3}\left[+V_{sat}-\left(-V_{ramp}\right)\right] \qquad 1$$

When affective voltage at point P

$$-V_{ramp}+\frac{R_2}{R_2+R_3}\left[+V_{sat}-\left(-V_{ramp}\right)\right]=0$$

$$-V_{ramp}+\frac{R_2}{R_2+R_3}V_{sat}+\frac{R_2}{R_2+R_3}V_{ramp}=0$$

$$-V_{ramp}\left[1-\frac{R_2}{R_2+R_3}\right]=\frac{-R_2}{R_2+R_3}V_{sat}$$

$$-V_{ramp}\left[\frac{R_3}{R_2+R_3}\right]=\frac{-R_2}{R_2+R_3}V_{sat}$$

$$-V_{ramp}=\frac{-R_2}{R_3}V_{sat}$$

When output of A_1 is $-V_{sat}$,

$$V_{ramp}=-\frac{R_2}{R_3}\left(-V_{sat}\right)$$

Peak to peak amplitude of triangular wave

$$V_o(pp)=+V_{ramp}-\left(-V_{ramp}\right)$$

$$=-\frac{R_2}{R_3}\left(-V_{sat}\right)-\left(-\frac{R_2}{R_3}V_{sat}\right)$$

$$=\frac{R_2}{R_3}V_{sat}+\frac{R_2}{R_3}V_{sat}$$

$$V_o(pp)\quad\frac{2R}{}V_{sat}$$

Time taking by the output to swing from $-V_{ramp}$ to $+V_{ramp}$ is equal to half time period T/2

$$V_o(pp) = \frac{-1}{R_1C_1}\int_0^{T/2}(-V_{sat})\,dt = \frac{V_{sat}}{R_1C_1}\frac{T}{2}$$

$$T = \frac{2\,R_1C_1V_o(pp)}{V_{sat}}$$

Sub the value of $V_o(pp)$

$$T = \frac{2\,R_1C_1\left(\frac{2R_2}{R_3}V_{sat}\right)}{V_{sat}} = \frac{4\,R_1C_1R_2}{R_3}$$

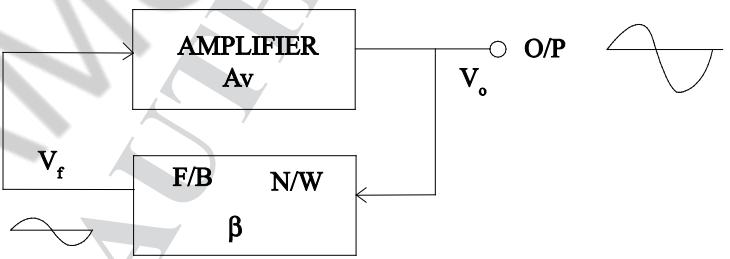
$$T = \frac{4\,R_1C_1R_2}{R_3}$$

$$f_o = \frac{1}{T} = \frac{R_3}{4\,R_1C_1R_2}$$

$$f_o = \frac{R_3}{4\,R_1C_1R_2}$$

8. Explain the Sine Wave Generators:

An oscillator is basically a feedback circuit where a fraction V_f of output voltage V_o of an amplifier is feedback to the input in the same phase.

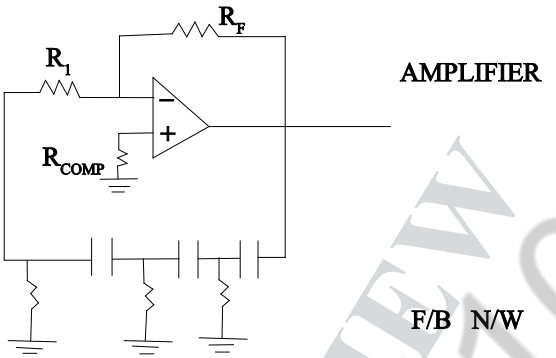


For sustained oscillation, $A_v\beta = 1$

$$|A_v\beta| = 1$$

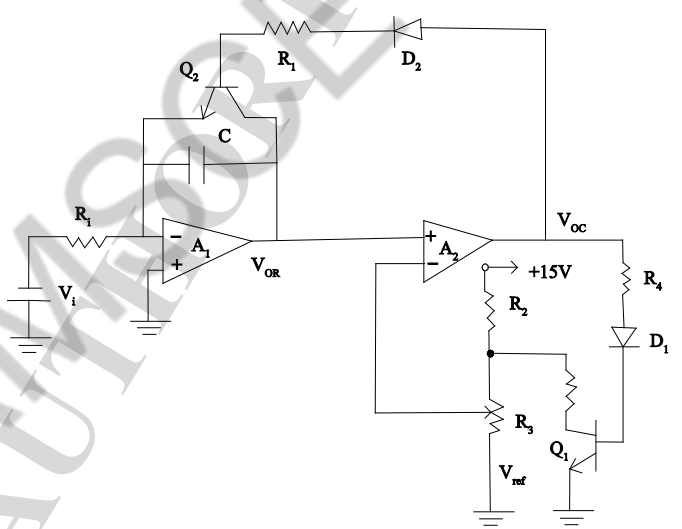
$$\angle A_v\beta = 0^\circ \text{ or } 360^\circ$$

Phase Shift Oscillator:



Amplifier provides a phase shift of 180°. Addition phase shift of 180° provided by Rc N/w.

9. Explain the Sawtooth Wave Generator:



Op-amp A_1 function as a ramp generator, A_2 will function as a comparator. −ve input voltage source is connected to the ramp generator. So the output will be +ve going ramp signal. This ramp voltage is connected to the (+) terminal of comparator A_2. And to the (−) terminal of comparator A_2, reference voltage is connected.

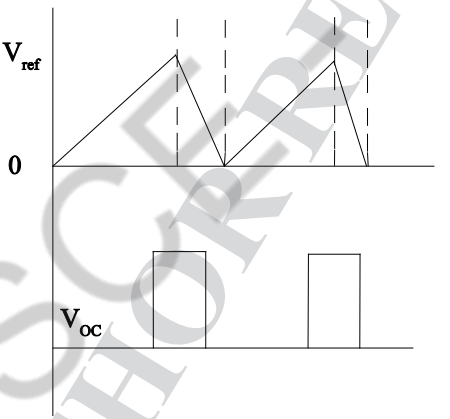
When the (+) going ramp signal becomes greater than the reference voltage, A_2 output will be +ve. This output will turn ON D_1, D_2, Q_1, Q_2. Due to this action, reference voltage will set to 0v and the capacitor path will be shorted.

Now, the capacitor will start to discharge. When the amplitude of discharging waveform, becomes less than 0v, again switching will take is place.

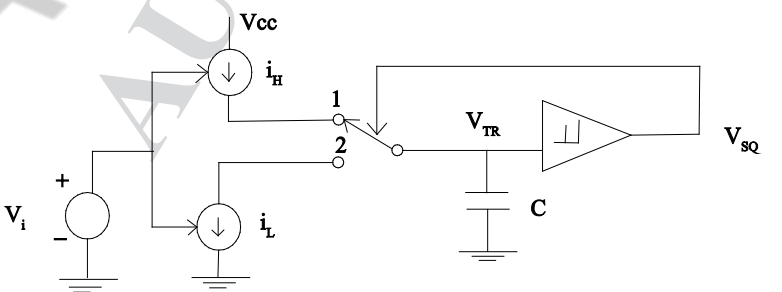
Cycle repeats.

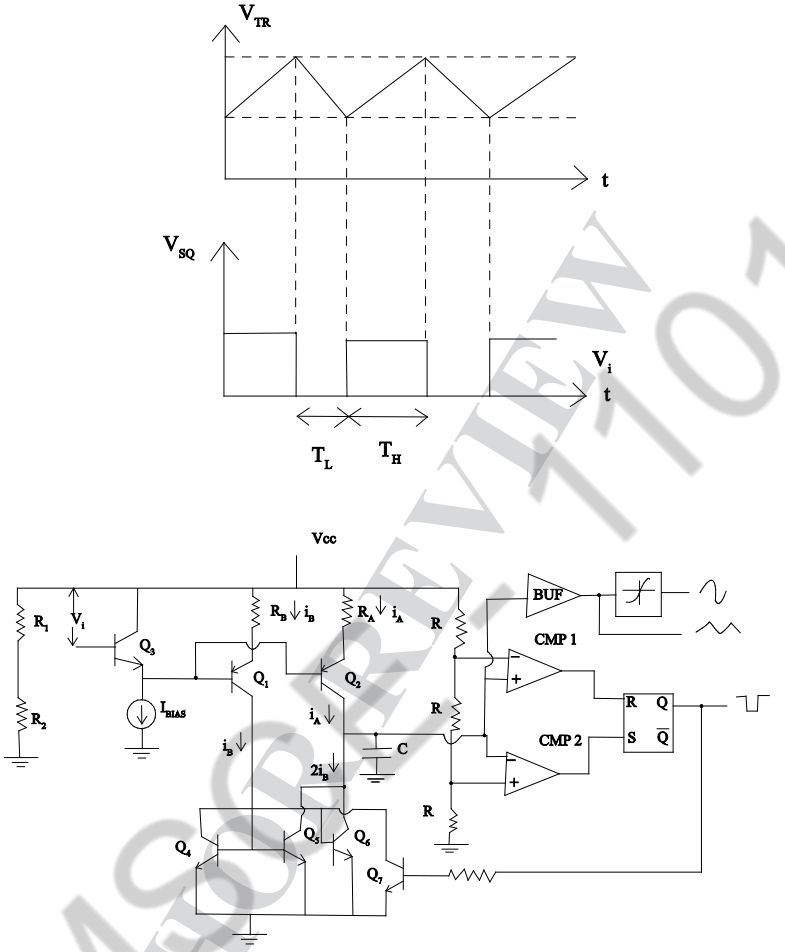
$$f = \left(\frac{1}{R_i\ C}\right)\frac{V_i}{V_{ref}}$$

$$f = \frac{I_s}{C\ V_{ref}}$$



10. Explain the ICL 8038 Function Generator:





Refer the 1st figure. When switch S is in position 1, capacitor charge at a rate fixed by current source i_H. When voltage V_{TR} across capacitor reaches the upper threshold of Schmitt trigger, it changes state and flips the switch to position 2. The capacitor now discharge through the current sink i_L. When voltage V_{TR} reaches the lower threshold of Schmitt trigger, it switch will change to position 1. This sequence will repeat cyclically.

Refer the 2nd figure.

Transistors Q_1 and Q_2 are 2 programmable current sources. Magnitude if current set by R_A and R_B. Emitter follower formed by the transistor Q_3 drives the bases of Q_1 and Q_2.

$$i_A = \frac{V_i}{R_A}; \quad i_B = \frac{V_i}{R_B}$$

Current i_A fed directly to the capacitor. Current i_B fed to the capacitor through the current mirror circuit. Current mirror is formed by Q_4, Q_5, Q_6. Schmitt trigger is formed by CMP1, CMP2, P – S F/F.

Assume output of F/F Q is HIGH. This will turn ON Q_7. As a result, bases of Q_5 and Q_6 will be connected to GND. This process will shunt the current sink OFF. Thus The capacitor will charge at a rate determined by $i_H = i_A$.

When the amplitude of charged capacitor becomes $V_{TH} = \frac{2}{3}Vcc$, CMP1 will trigger. This will reset the F/F. Thus Q = 0(LOW). This (Q = 0) output will turn OFF Q7. Now, Q_4, Q_5, Q_6 will act as current mirror.

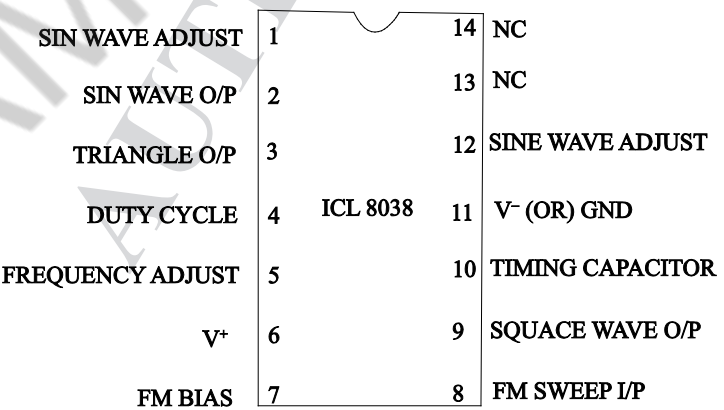
$$i_C = 2i_B - i_A$$

Since $2i_B > i_A$, capacitor continues to discharge. Once V_{TL} is reached, CMP2 triggers and it will set the F/F. Thus the cycle repeats

$$f_o = 3\left(1 - \frac{R_B}{2R_A}\right)\frac{V_i}{R_A C\, Vcc}$$

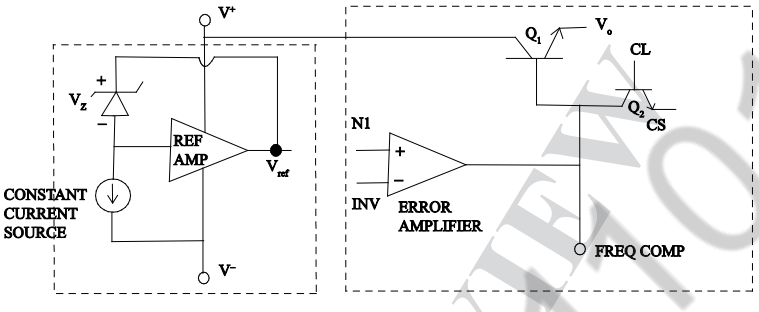
When $R_A = R_B = R$

$$f_o = KV_i \quad \text{where} \quad K = \frac{1.5}{RcVcc}$$



11. With neat example, explain the IC 723 General Purpose Linear Voltage Regulator:

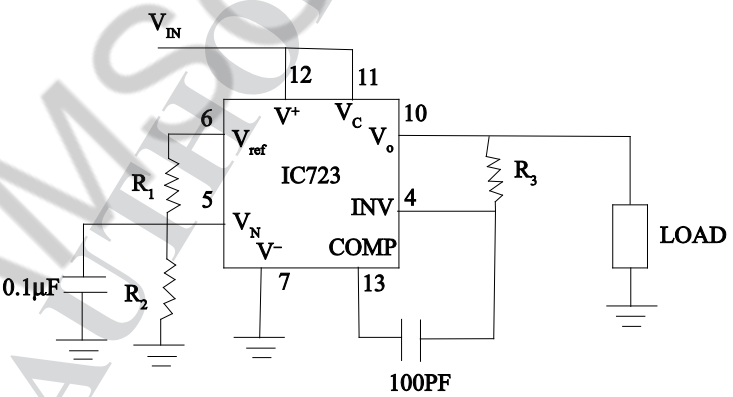
Internal Diagram of IC 723

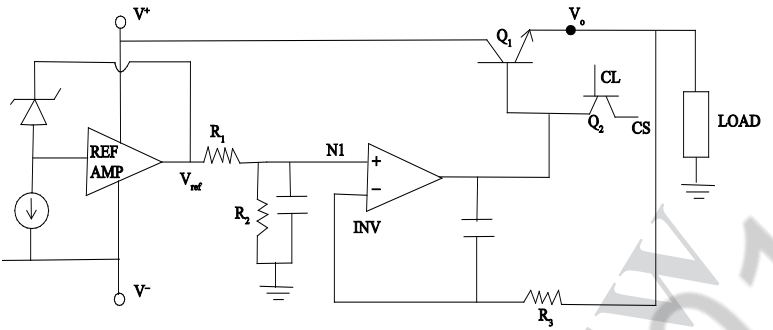


IC 723 consist of sections. Zever diode, constant current source, reference amplifier used to produce a fixed voltage of 7 volts. Constant current source forces the zever to operate at a fixed voltage.

The other section consist of error amplifier, series phase transistor, current limit tarasistor.

Low Voltage Regulator Using IC 723





Using the reference section, reference voltage V_{ref} is generated. V_{ref} Is connected to NI terminal of error amplifier through R1R2 divider network

$$\therefore \quad V_{NI} = V_{ref} - \frac{R_2}{R_1 + R_2}$$

Another input to the error amplifier is given from the output terminal V_o. Difference between two signals is amplified by the error amplifier. output of error amplifier will drive the series pass transistor Q_1 so as to minimize the difference b/w NI and INV input.

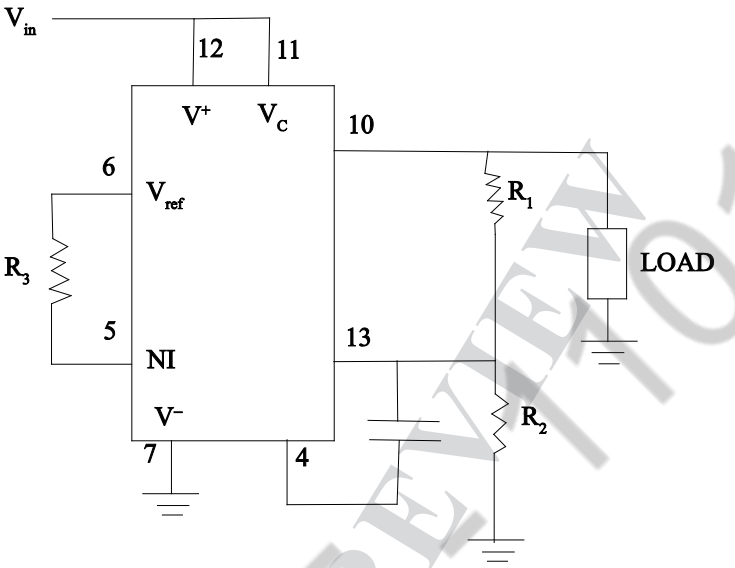
Since Q_1 act as emitter follower

$$V_o = V_{ref} \frac{R_2}{R_1 + R_2}$$

$$V_o = 7.15 \frac{R_2}{R_1 + R_2} \qquad \left[\because V_{ref} = 7.15v\right]$$

Suppose if output voltage becomes low, inverting input also will become low. So the error amplifier output ie ($V_{NI} - V_{INV}$) will go high. This will cause the transistor to conduct heavily. More current will flow through the load. Thus the initial drop in load voltage has been compensated by the increase in output voltage.

12. Describe the High Voltage Regulator Using IC 723:



Since the NI terminal connected directly to V_{ref},

$$V_{NI} = V_{ref}$$

$$\therefore \quad A = 1 + \frac{R_F}{R_i}$$

$$V_o = \left(1 + \frac{R_F}{R_i}\right) V_i$$

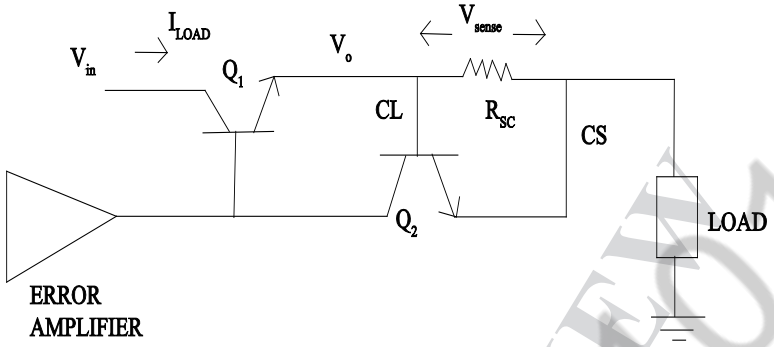
$$V_o = \left(1 + \frac{R_1}{R_2}\right) V_{ref}$$

Hare $V_i = V_{ref}$

$R_F = R_1$

$R_2 = R_i$

Current Limit Protection IN IC 723

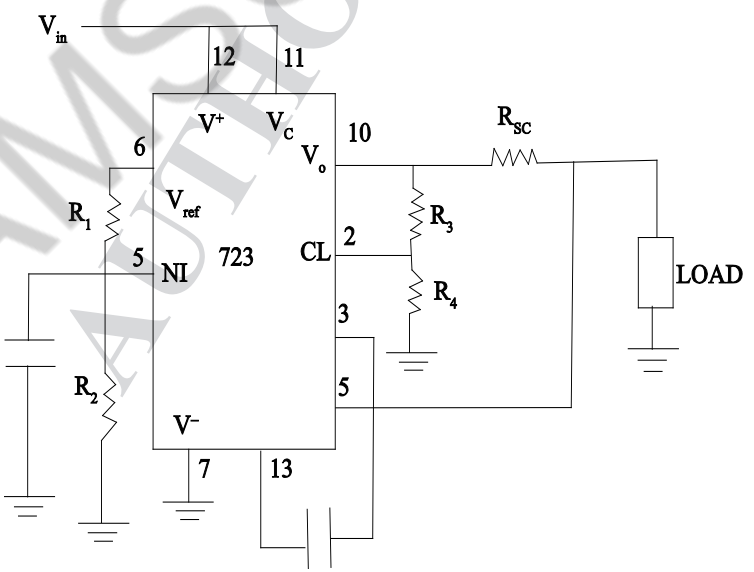


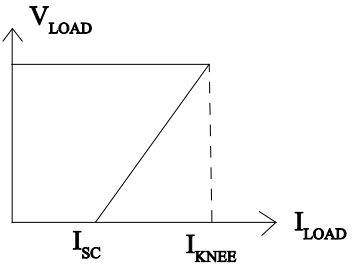
Current limiting refers to the ability of a circuit to increases above a present value. Resistor R_{SC} is connected b/w CL & CS terminal. Under short circuit condition, I_L will be high. So the drop across the R_{SC} will be high. This will turn ON Q_2.

So the part of current from error amplifier will divert to Q_2, thus reducing the I_B of Q_1. This in turn will decrease I_B of Q_1. Thus the load current will get reduced.

Current Fold Back Method Using IC 723

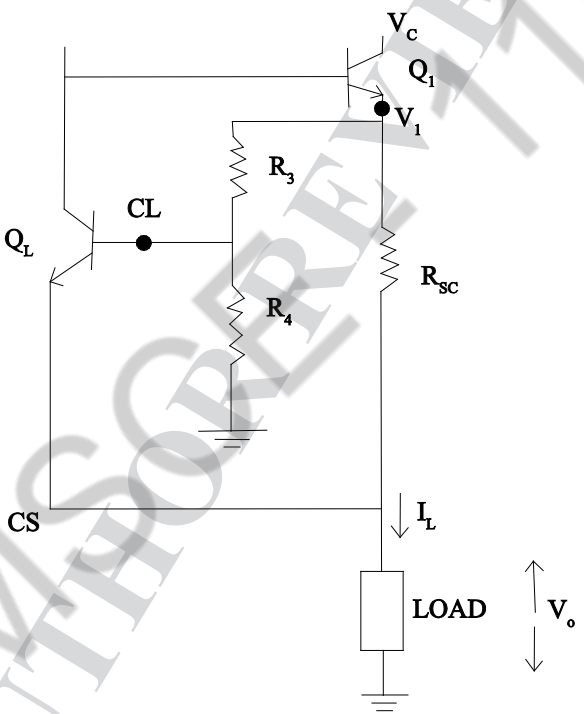
This is a method which will limit the short circuit current get allow higher current to the load.





Upto I_{KNEE}, V_L was constant.

When the current tries to exceed I_{KNEE}, both V_L, I_{LOAD} get decreased.



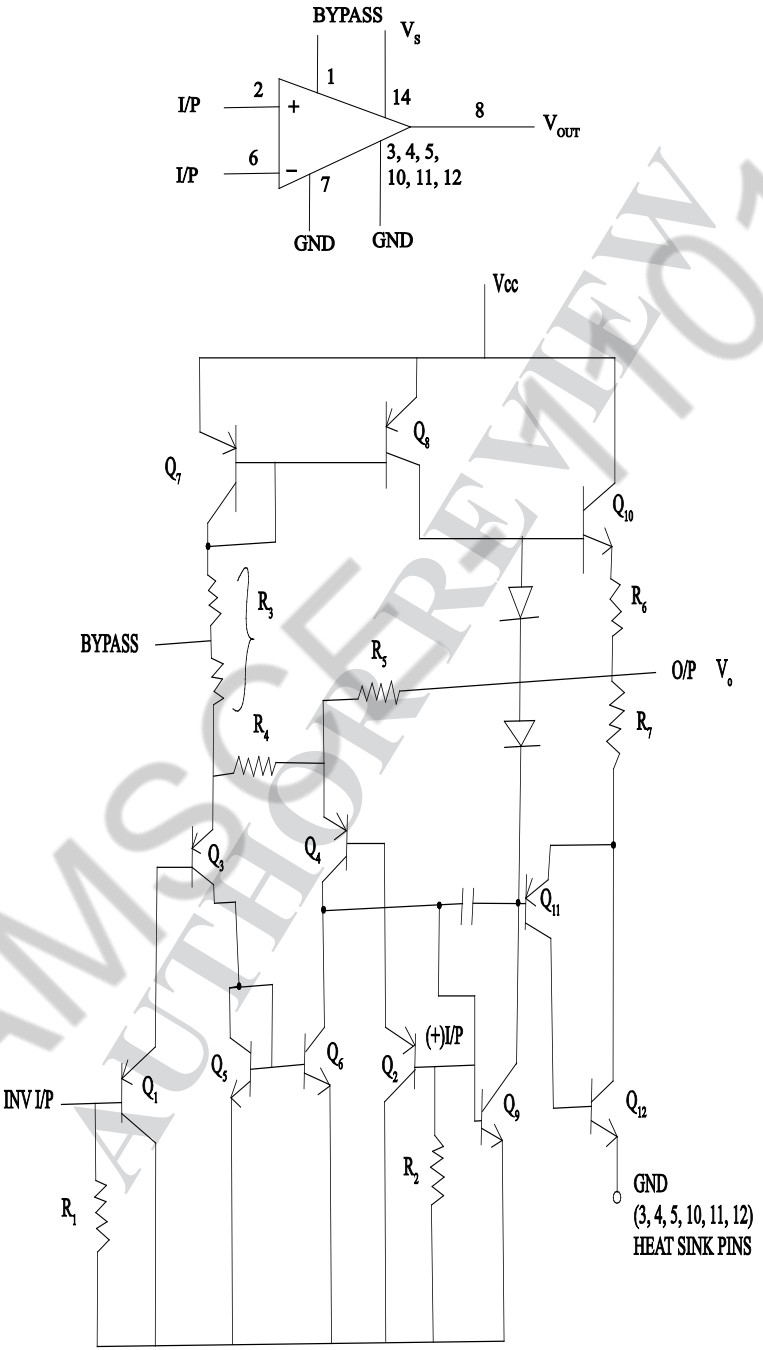
Voltage at CL is divided by R_3 and R_4. Q_2 will turn ON only when drop across R_{SC} is large.

If Q_2 turns ON, Q_1 will OFF. This will reduce V_1, V_o, I_L

$$V_{CL} = V_1 \frac{R_4}{R_3 + R_4}$$

This process continue till $V_o = 0v$

13. Explain LIT 380 Audio Power Amplifier:



It consist of 4 stages

i) PNP emitter follower

ii) Differential amplifier

iii) Common emitter amplifier

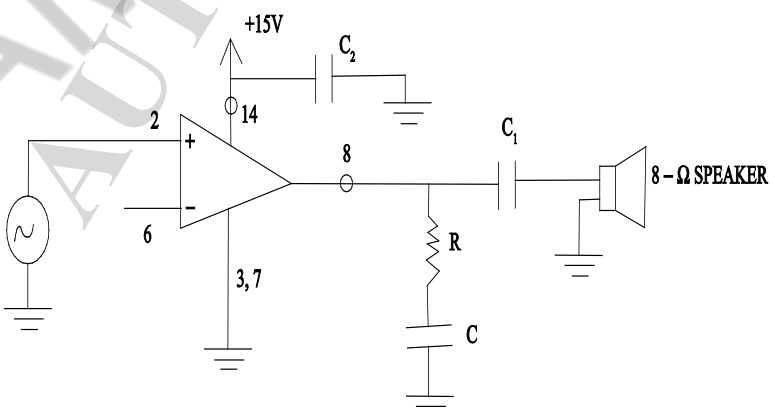
iv) Quasi complimentary emitter follower

Transistors Q_1 and Q_2 forms the PNP emitter follower. The output of Q_1 and Q_2 is used to drive the differential pair formed by the transistors Q_3 and Transistor Q_5 and Q_6 act as collector load for differential pair Q_3 – Q_4. Transistor Q7 and the resistor R3 determine the biasing current of differential pair $Q_3 – Q_4$. Transistor Q_7 and Q_8 forms another current and it delivers a collector current of Q_9. Single ended output taken at the collector of Q_8 and it is given as input to the lease of transistor Q_9.

Transistor Q_9 act as common emitter amplifier capacitor connected between base and collector Q_9 provides the internal compensation. Transistor Q_{10} and Q_{12} forms the Quasi – complier emitter follower stage. Feedback is introduced to the emitter of Q_4 the resistor R_5 to stabilize the output.

Feathers:

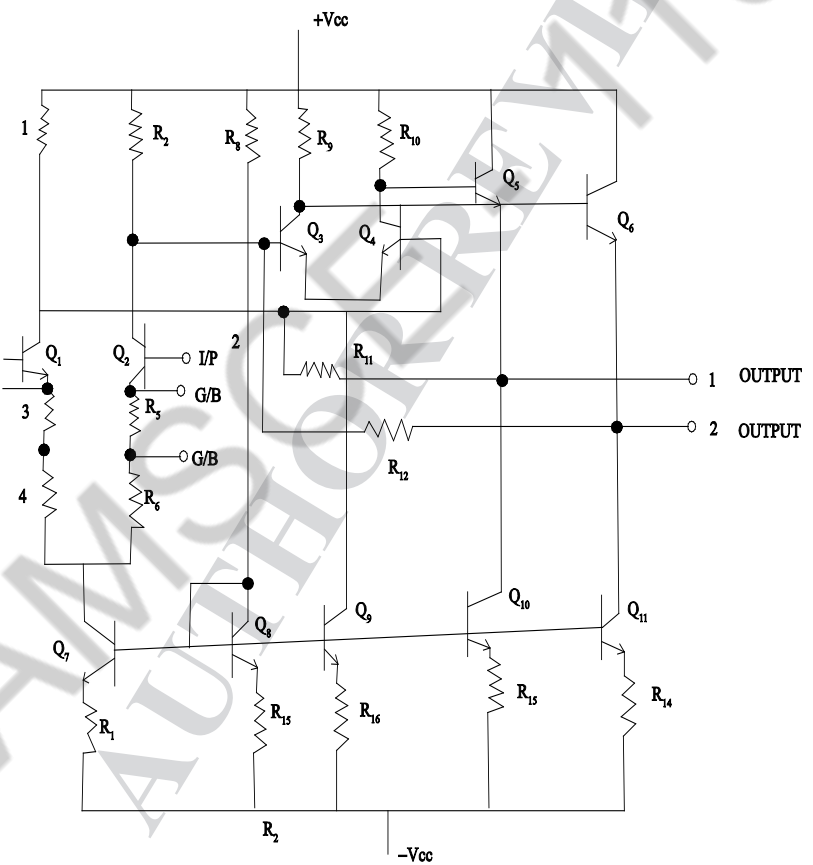
1. Supply voltage range is from 5v to 20v
2. Voltage gain of 34dB
3. High input impedance – 150KΩ
4. Bandwidth – 100KHz
5. Maximum current – 1.3A
6. Low distortion – 0.2 of



The IC is used in non - inverting made. Inverting terminal can be connected to GA or it may left open. Capacitor C2 is used to decouple the power supply. Rc network is added to improve the stability. This eliminates 5 to 10 MHz oscillation in an RF sensitive environments.

14. Explain the Video Amplifier:

Video amplifier is designed to achieve a flat in V_s frequency. Per television applications, bandwidth requirement of the order of 4 – 6 MHz. for such high bandwidth applications, video amplifier can used. Technique involved to obtain large bandwidth is off gain for increased bandwidth. Feedback is employed for this purpose.



It consist of

1. Two cascaded BIT differential amplifier
2. Balanced emitter follower stage

Wide bandwidth is achieved by the use of low value load resistance for the two differential amplifier stages and the use of internal feedback loops. Transistors Q_1, Q_2 and the load resistors R_1, R_2 forms the input differential stage. Q_7 provides current sinking biasing for the first differential stage.

Q_3, Q_4 forms the second differential stage, R_9. Act as load resistors for the second differential stage. Transistor Q_9 provides the current sink bias. output of second differential stage is used to drive the emitter followers realized by Q_5 and Q_6, Q_{10} and Q_{11} act as current sink bias for the emitter follower stages. Resistors R_3, R_4, R_5, R_6 provides negative feedback within first stage. Resistors R_{11}, R_{12} provides negative feedback from the output terminals to the balanced input terminals of second stage.

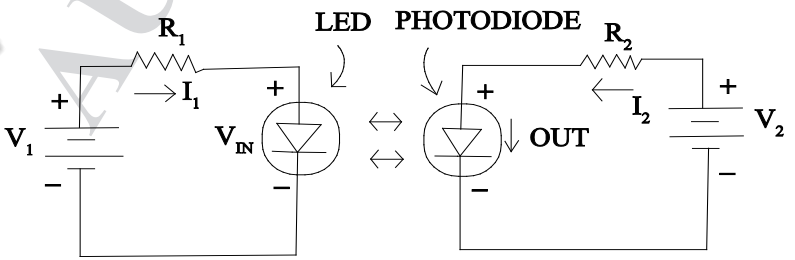
Diode connected transistor Q_8 along with resistors R_8 and R_{15} provides the biasing to Q_7, Q_9, Q_{10}, Q_{11}. Gain adjustment can be done by modifying the amount of series F/B connected in the first stage. For this purpose, resistor taps (G_{1A}, G_{2A}) and (G_{1B}, G_{2B}) are used.

Features:

1. Wide Bandwidth – 120 MHz
2. INPUT Resistance – 250 KΩ
3. Gains of 10, 100, 400 are selectable
4. External frequency compensation is not requires
5. High CMRR

15. Explain Optocoupler/Optoisolator:

An ortocoupler is a solid state complement in which the light emitter light path and light detector are all enclosed within the component and can't be changed from outside. As the ortocoupler provides electric isolation between two circuits, it is also called an Orto isolator.



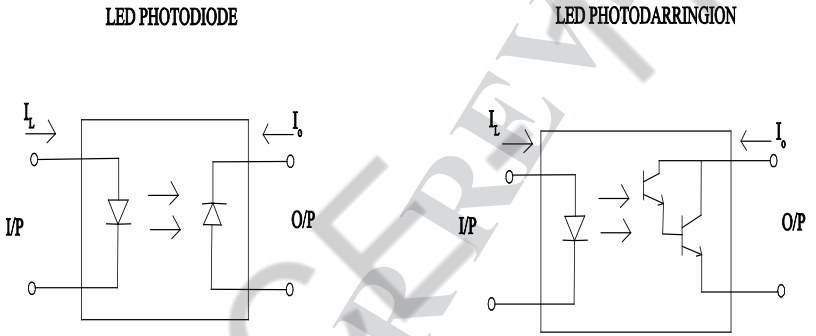
Source V_1 and series resistance R_1 decide the forward current I_1 through the LED. Thus the LED will emit light. When the emitted light incident on photodiode, reverse current will set in the output circuit. Due to the reverse current, voltage will be dropped across the resistor R_2.

Thus $V_{OUT} = V_2 - I_2R_2$

Now if input is changed, the amount of light emitted ley LED will change. This will change the output voltage.

Types of Opto Coupler:

1. LED Photodiode
2. LED Photo Darlington



MOC 3009 - MOC 3012

Characteristics of Opto Coupler:

Current Transfer Ratio (CTR):

$$CTR = \frac{I_C}{I_F} \times 100\%$$

Isolation Voltage Between INPUT and OUTPUT (Visc):

Isolation voltage is another factor in choosing a photo coupler. This is because, photo couplers are used for angle transmission between circuits

that have different potential, which tend to generative impulsive voltage. Isolation voltage is specified in KV_{rms}.

Response Time:

It depends on

1. output photo transistor
2. input forward current
3. Load resistance

Bandwidth:

20 KH_Z – 500 KH_Z

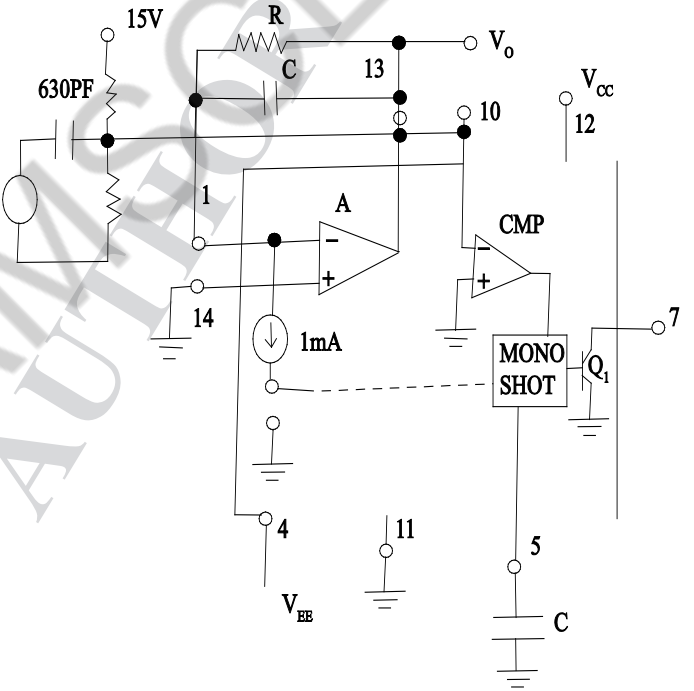
$I_{L(max)}$:

Max permissible d.c current = 40 mA – 100 mA

VCE (max):

Max allowable d.c voltage that can be applied to output photodiode.

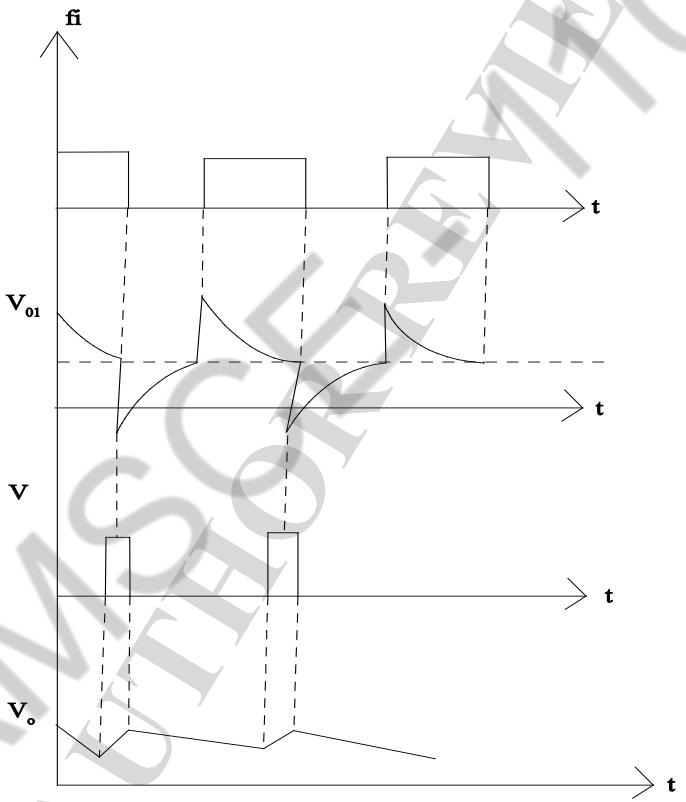
16. Explain the Frequency to Voltage Converter:



output frequency to voltage converter produces an output voltage whose amplitude is a function of frequency of input signal.

$$V_o = K_F \text{ fi}$$

The input frequency is applied to the comparator CMP and the output is derived from op-amp A. For input pulse, output V_{01} will be positive and negative spikes. For each negative spike, comparator CMP triggers the one shot multivibrator. The output of multivibrator will close the switch sw, pulling IMA out of Ci for the duration T_H. This action will increase V_o.



Assume f_i be the input frequency

Thus pulsed current $I = f_i \times 1\text{mA} \times T_H$

$$V_o = I \times R$$

$$V_o = 10^{-3} \times T_H \times R \times f_i$$

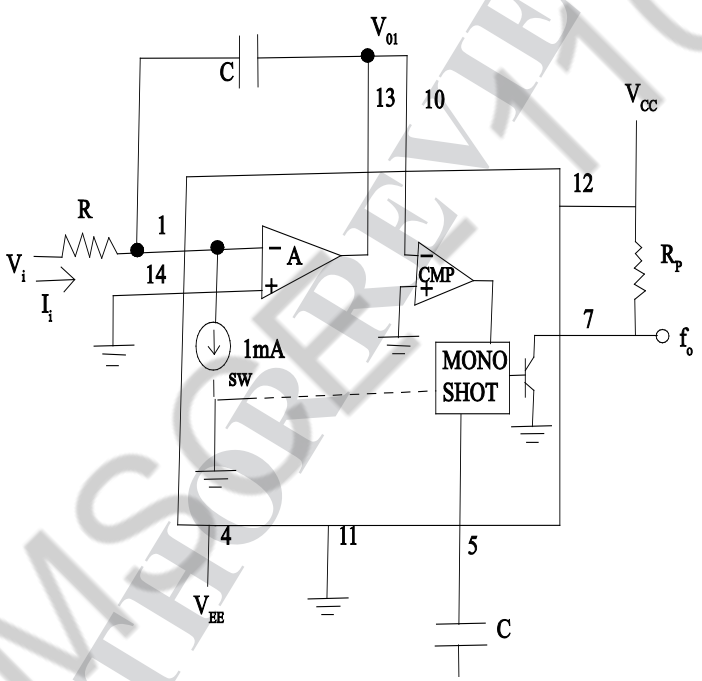
$$T_H = \frac{CV_i}{I} = \frac{C \times 7.5}{1 \times 10^{-3}}$$

$V_o = 7.5\ RC\ f_i$

17. Explain the Voltage to Frequency Converter Using VFC 32:

Voltage to frequency converter produces an output signal whose frequency is a function of external control input voltage.

$$f_o = K_o V_i$$



The op-amp A converts the input V_i to a current I_i

$$I_i = \frac{V_i}{R}$$

When the switch is open, current I_i will flow into the capacitor. When the switch is closed, current I_i will flow into the capacitor. When the switch is open, current I_i will flow into the capacitor. This will cause V_{01} to ramp downwards. When V_{01} reaches zero, comparator triggers and sends a

triggering signal to one shot multivibrator that closes the switch sw and also turns the transistor Q ON for a time interval T_H set by capacitor C.

$$T_H = \frac{75 \times C}{1 \times 10^{-3}}$$

When the switch closes, currents will flow out of capacitor. This will cause V_{01} to ramp upwards.

$$\Delta V_{01} = (1mA - I_i) T_H / C_i$$

Time duration T_L taken for V_{01} to return to zero,

$$T_L = \frac{C_i \Delta V_{01}}{I_i}$$

$$I_i T_L = C_i \Delta V_{01}$$

$$= \frac{C_i (1mA - I_i) T_H}{C_i}$$

$$= (1mA - I_i) T_H$$

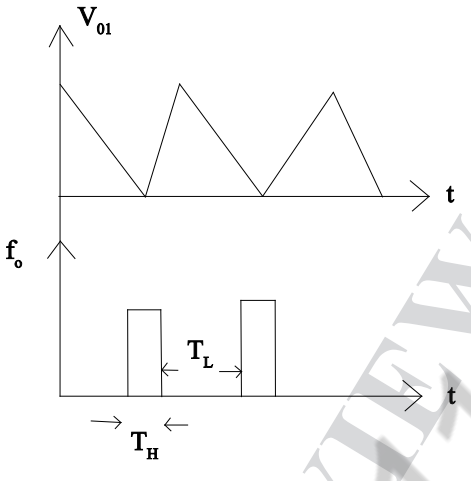
$$I_i (T_L + T_H) = (1mA) T_H$$

$$T_L + T_H = \frac{(1mA) T_H}{I_i}$$

Where $I_i = \frac{V_i}{R}$

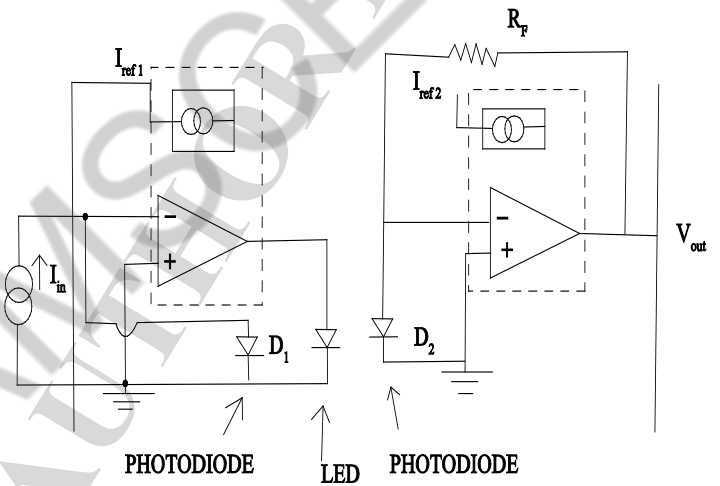
$$f_o = \frac{1}{T_L + T_H} = \frac{I_i}{(1mA) T_H} = \frac{V_i}{1 \times 10^{-3} \times R \times 7.5 \times C} \times 10^{-3}$$

$$f_o = \frac{V_i}{75CR}$$



18. Explain the Isolation Amplifier

An isolation amplifier is an amplifier that offers an ohmic or electrical isolation between its input and output terminals. They can provide voltage difference of several thousands of volts between input and output.



LED and a pair of photo-diode are coupled together to isolate the output signal from the input. LED and photo-diode are arranged such that same amount of light balls on each photo-diode. I_{ref1}, and I_{ref2} are required to generate a midscale reference. Negative feedback around A_1 occurs through optical path formed by the LED and D_1. Signal is transferred across the

isolation barrier by the matched light path to D_2. As the LED light output increases, D_1 responds by generating an increased current.

The current increases until the sum of currents in and out of the input node is zero. At that point, negative feedback through D_1 has stabilized the loop.

Thus $I_{D1} = I_{IN}$

Since D_1 and D_2 are matched, $(I_{D1} = I_{D2})$

$$I_{D2} \simeq I_{IN}$$

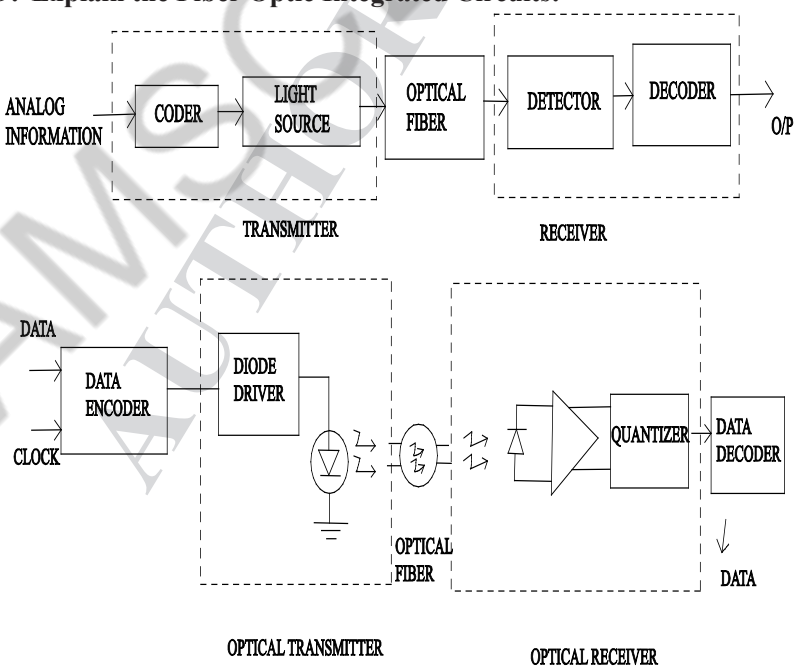
Current produced by D_2 must either flow into A_2 or R_F. Since, A_2 is designed for low bias current almost all the current will flow through R_F.

So $V_o = I_{D2} R_F \simeq I_{IN} R_F$

Features:

1. Wide Bandwidth = 60 KHz
2. 750V continuous isolation voltage
3. Ultra low leakage: 0.3 μA, max at 240v/60Hz
4. 18 pin D/P package

19. Explain the Fiber Optic Integrated Circuits:



Consider an example of point to point telecommunication systems. In this, telephone user is transmitting analog information. Thus the transmitter telephone is the source of analog information. With the help of coder, analog signal is converted to digit. Such digital data is then coded to pulses of light.

The light pulses are transmitted to the receiver through the optical filter. The light pulses are guided by the process called total interval reflection. The receiver converts the optical pulses to electrical signal and then it is decoded to analog signal using decoder. When light propagates along filter, it will experience delay distortion and attenuation.